Jetson TX2 NX Tuning and Compliance Guide

Application Note

Document History

DA-10383-001_v1.2

Version	Date	Description of Change
1.0	February 24, 2021	Initial Release
1.1	April 20, 2022	• Minor addition to the "PCIe Compliance Testing" section • Added two file attachments
1.2	May 4, 2022	Added "Jetson TX NX HDMI Compliance Testing" section

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Jetson TX2 NX USB2.0 Tuning Guide

This chapter describes the registers and steps needed to tune the USB2.0 high speed eye diagram for NVIDIA® Jetson™ TX2 NX. USB-IF provides complete test specification and instructions on their website (https://www.usb.org) for high-speed host and device mode testing. NVIDIA typically uses Tektronix oscilloscopes for USB characterization.

Customers are free to use oscilloscopes from other vendors to do USB characterization.

> **Note**: Jetson TX2 NX uses NVIDIA Tegra X2 which is a Parker series system on chip (SoC).

Equipment

The components required to perform USB2.0 tuning includes:

- ▶ Tektronix TDS694C or faster digital sampling oscilloscope
- ▶ Tektronix P6247 or P6248 or equivalent differential probe x1
- ▶ High-speed USB electrical test fixture, available from USB-IF
- ▶ Tektronix oscilloscope USB test software
- ▶ Tool to access register/memory space in Tegra or build a special image to force USB test mode enabled (for example, devmem2 can be used in Linux environment)

Registers for Host Mode Testing

Figure 1 shows the relationship between the USB ports and the xUSB controllers.

Figure 1.   Tegra X2 USB Controllers and Interface Routing Map
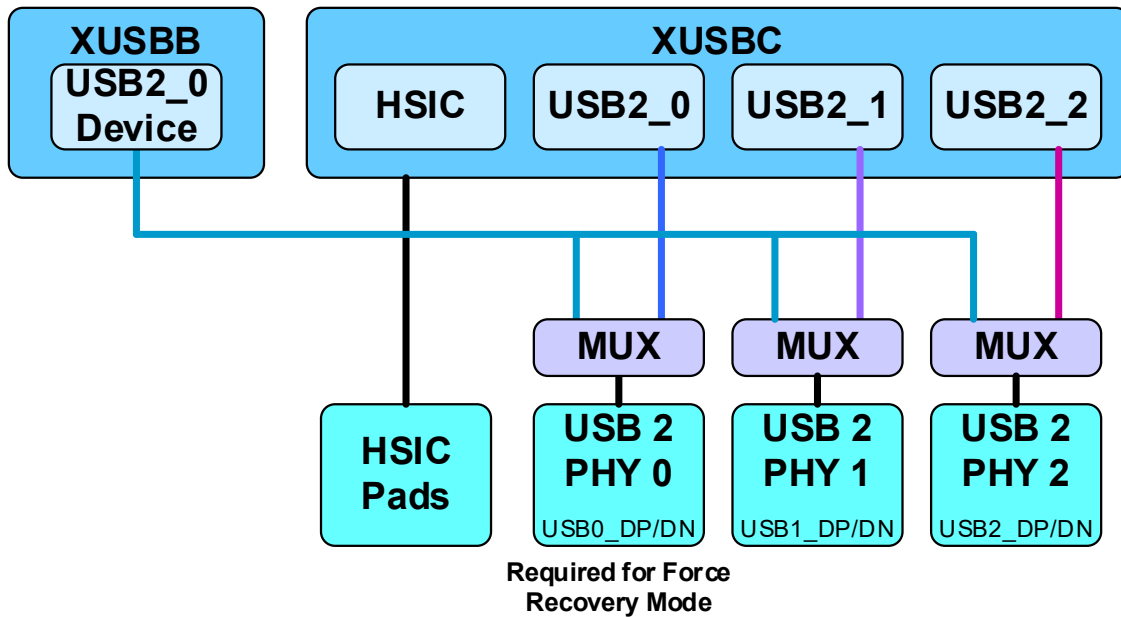

Figure 2.   Jetson TX2 NX USB Connection Example
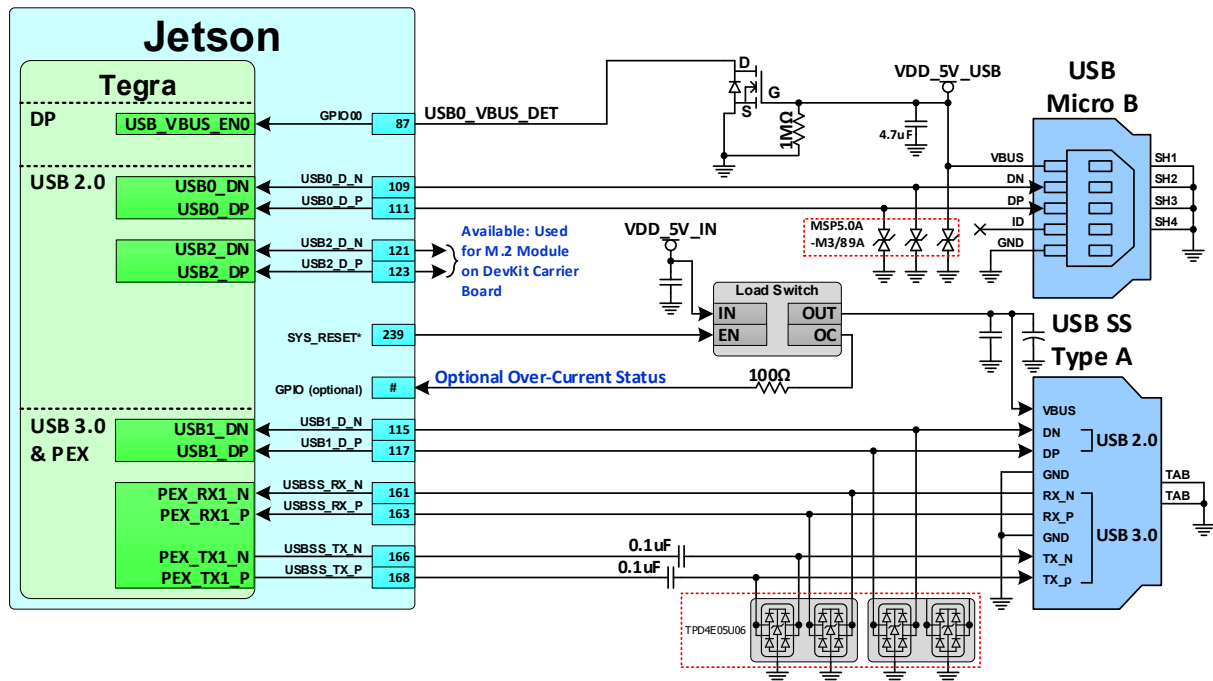
Toggle the Jetson TX2 NX USB registers listed in Table 1 to force Test J, Test K, Test SE0 NAK, and Test Packet on the respective USB port.

Table 1.   xUSB USB2.0 Port Test Control Registers

Descriptions	Register Name and Setting
Normal Operations (default)	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0000b
Test J	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0001b
Test K	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0010b
Test SE0 NAK	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0011b
Test Packet	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0100b
Force enable	XUSB_XHCI_OP_PORTPMSCHS_x_TM [31:28] = 0101b

xUSB USB2.0 Port Registers Address:

▶ USB0: 0x03530454: XUSB_XHCI_OP_PORTPMSCHS_3
▶ USB1: 0x03530464: XUSB_XHCI_OP_PORTPMSCHS_4
▶ USB2: 0x03530474: XUSB_XHCI_OP_PORTPMSCHS_5

Test Mode Programming Sequence

The programming sequence for enabling USB2.0 test mode is as follows:

> **Notes**: The output of USB2.0 test pattern is only supported for point-to-point connections.
>
> The phrase "any USB device" refers to any real device, such as HS USB flash drive or LS mouse.

1. Connect any USB device to the port (this will prevent the controller from entering power down mode).
2. Disable the auto-suspend for the controllers:

   a). For example: the following command under Linux Kernel.

   echo on > /sys/bus/usb/devices/usb1/power/control

> **Notes**: "usb1" is the XHCI USB2 controller; it may map to "usb2" if there is another USB controller on the board. The XHCI bus number can be found under /sys/devices/3530000.xhci/.

3. Set PP (Port Power) in Disabled state by XUSB_XHCI_OP_PORTSC* bit [9] = 0.

       USB0: 0x03530450: XUSB_XHCI_OP_PORTSC_3

       USB1: 0x03530460: XUSB_XHCI_OP_PORTSC_4

       USB2: 0x03530470: XUSB_XHCI_OP_PORTSC_5

4. Set RS (Run/Stop) bit in the XUSB_XHCI_OP_USBCMD_0 bit [0] = 0.

        0x03530020: XUSB_XHCI_OP_USBCMD_0

5. Wait for the HCHalted (HCH) bit in the XUSB_XHCI_OP_USBSTS_0 bit [0] = 1.

   0x03530024: XUSB_XHCI_OP_USBSTS_0

6. Set the xUSB Port Test Control registers in PORTPMSCHS register (see Section "Registers for Host Mode Testing"

> 📝 **Note**: Per USB2.0 Specification, only a single downstream facing port can be in test_mode at a given time.

7. Disable Pad PD (power down) by clearing the XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0 bit [26] = 0.

   USB0: 0x03520088: XUSB_PADCTL_USB2_OTG_PAD0_CTL_0_0

   USB1: 0x035200C8: XUSB_PADCTL_USB2_OTG_PAD1_CTL_0_0

   USB2: 0x03520108: XUSB_PADCTL_USB2_OTG_PAD2_CTL_0_0

8. Plug in the test fixture to start USB2.0 eye diagram test.

> 📝 **Note**: In steps 3, 6, and 7, USB0 is USB0_D+/D- (Pin # 111/109), USB1 is USB1_D+/D- (Pin # 117/115), and USB2 is USB2_D+/D- (Pin # 123/121).

Registers to Adjust High Speed USB2.0 Eye Diagram

The following are Jetson TX2 NX USB registers that may be needed to tune the USB2.0 eye diagram. Refer to the "Tuning Procedure" section on how to use these registers during characterization.

Table 2.   xUSB Registers

Register Name	Bit Fields	Description
XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0: Address 0x03520088 for USB0, 0x035200C8 for USB1, and 0x03520108 for USB2		
HS_SLEW (See Note 1)	8:6	HS slew rate control
HS_CURR_LEVEL (See Note 2)	5:0	HS driver output setup control
XUSB_PADCTL_USB2_OTG_PADx_CTL_1_0: Address 0x0352008C for USB0, 0x035200CC for USB1, and 0x0352010C for USB2		
RPD_CTRL	30:26	RPD_CTRL (15K host pull down)
TERM_RANGE_ADJ	6:3	HS termination control
XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0: Address 0x03520284		
HS_SQUELCH_LEVEL (See Note 3)	2:0	HS SQUELCH control for device RX testing

Register Name	Bit Fields	Description
XUSB_PADCTL_USB2_OTG_PADx_CTL_3_0: Address 0x03520094 for USB0, 0x035200D4 for USB1, 0x03520114 for USB2		
HS_RXEQ	8:6	HS_RXEQ (device RX testing)
HS_TXEQ	3:1	HS_TXEQ (device TX testing)
Notes:		

1. HS_SLEW where 0'b000 = slowest and 0'b111 = fastest
2. HS_CURR_LEVEL where 0'b000000 = highest current level and 0'b111111 = lowest current level
3. HS_SQUELCH_LEVEL where 0'b000 = lowest and 0'b111 = highest
4. The USBx is based on the module pin name, so USB0 is USB0_D+/D- (Pin # 111/109), USB1 is USB1_D+/D- (Pin # 117/115), and USB2 is USB2_D+/D- (Pin # 123/121).

Tuning Procedure

During chip production, each NVIDIA Tegra device is calibrated and the fuses corresponding to USB drive strength (HS_CURR_LEVEL), HS termination (TERM_RANGE_ADJ), and 15K host pull down (RPD_CTRL) are burnt on each chip.

Before making any USB measurements, ensure that the values programmed during production are loaded for HS_CURR_LEVEL, TERM_RANGE_ADJ and RPD_CTRL values into the pad configuration inputs.

To find out the default values, read from FUSE_USB_CALIB_0 fuse and FUSE_USB_CALIIB_EXT_0 fuse. See Table 3 for details.

Table 3.   FUSE_USB Registers

Register Name	Bit Field	Description
FUSE_USB_CALIB_0 (Address 0x038201F0)		
USB_CALIB	22:17	HS_CURR_LEVEL for USB2
USB_CALIB	16:11	HS_CURR_LEVEL for USB1
USB_CALIB	10:7	TERM_RANGE_ADJ for all USB ports
USB_CALIB	5:0	HS_CURR_LEVEL for USB0
FUSE_USB_CALIB_EXT_0 (Address 0x03820350)		
USB_CALIB_EXT	4:0	RPD_CTRL for all USB ports

During the characterization stage, manually adjusting the HS_CURR_LEVEL value should be enough to meet compliance requirements. It is possible to try and increase termination as a last resort.

> **Note**: NVIDIA does not recommend customers adjusting termination values. Do note that if the TERM_RANGE_ADJ needs to be adjusted, it may result in an impedance mismatch on the board and further attention may be needed.

It must be emphasized that if any HS_CURR_LEVEL modification is needed; it must be done as an offset to the default fused value since each device may have a different HS_CURR_LEVEL default value.

Do not apply a global overwrite HS_CURR_LEVEL value for all silicon. There is a mechanism provided in software to read fused USB drive strength and add an offset to it.

Pre-emphasis (EQ function) can also be tweaked for certain channel designs in addition to tweaking HS_CURR_LEVEL. EQ function can also help with long cable loss. To modify the EQ, write directly to XUSB_PADCTL_USB2_OTG_PADx_CTL_3_0 bits [8:6] for HS_RXEQ and [3:1] for HS_TXEQ.

Table 4.   EQ Function

HS_TXEQ[2:0]	AC Gain	HS_RXEQ[2:0]	SQ Level
00	+0 dB (default)	00	-0 dB (default)
01	+1.3 dB	01	-1.2 dB
10	+2.5 dB	10	-2.0 dB
11	+3.5 dB	11	-3.5 dB

Squelch is used to tune the RX sensitivity level - higher DCR loss will require a lower squelch level. To modify the squelch level, write directly to XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0 bits [2:0].

Lastly, the slew rate can be modified by writing directly to XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0 bits [8:6].

HS_CURR_LEVEL Offset Adjustment Procedure

If the default value does not fit customer design, adjust the HS_CURR_LEVEL register to pass USB HS eye diagram. Follow these steps for tuning:

1. Obtain default value; read reg. ˝FUSE_USB_CALIB_0˝(Address: 0x038201F0) :
    a). USB_CALIB [5:0]: USB pad HS_CURR_LEVEL[5:0] for USB0

    b). USB_CALIB [16:11]: USB pad HS_CURR_LEVEL[5:0] for USB1

    c). USB_CALIB [22:17]: USB pad HS_CURR_LEVEL[5:0] for USB2

2. Calculate offset from fused HS_CURR_LEVEL value and desired value to pass eye mask.

    a). For example, if default value as 0x20, and desired value as 0x1C, where offset = -4

    b). For example, if default value as 0x10, and desired value as 0x14, where offset = +4

3. Adjust HS_CURR_LEVEL register as described in the "Tuning Procedure" section.

    a). Maximum allowable offset: ±6 steps

Provide the "tuned offset steps" to software team.

Software Verification

A functional check is recommended. Connect the DUT to USB hosts and devices to perform a check on functionality.

To check if software implements the tuned offset step properly, load new software with offset included into another DUT and check to ensure:

HS_CURR_LEVEL = USB_CALIB + tuned offset steps

Jetson TX2 NX USB SS Compliance Test Guide

This chapter serves as the high-level guide to compliance testing of the SuperSpeed USB (5 Gbps) PHY in Jetson TX2 NX. The Jetson TX2 NX Developer Kit has been tested for USB specification compliance and passed under worst case scenarios. Therefore, no tuning will be required if customer designs follow routing guidelines published in our design guides.

Compliance Testing

The *Electrical Compliance Test Specification for SuperSpeed Universal Serial Bus* Rev 0.79 provides the compliance criteria and test descriptions for SuperSpeed USB devices, hubs, and host controllers that conform to the *Universal Serial Bus 3.0 Specification*, Rev 1.0. Customers should refer to the document for a high-level overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure to perform the test.

Placing Jetson TX2 NX in Compliance Mode

To run the TX electrical compliance test, the Jetson TX2 NX must be placed in compliance mode. Perform the following 2 steps to achieve this.

1. Disable runtime power management for USB Host Controller.
2. Set CTE = 1 in PORTSC.

Linux for Tegra Image

1. Boot up the DUT (ensure the USB3.0 Host Test Fixture is not connected to the DUT).
2. Install the latest Linux for Tegra Image.
3. Run the following script to disable power management for USB Host Controller.

```
!/bin/sh
for hub in $(ls -d /sys/bus/usb/devices/usb?); do
echo on > $hub/power/control
done
```

4. Install the devmem tool by running the following command.

```
$ sudo apt-get install devmem2
```

5. Set CTE = 1 in PORTSC by writing Ah to XUSB_XHCI_OP_PORTSC[8:5].

```
devmem2 0x03530430 w 0x10340  // USB_SS#1
```

> 💬 **Notes**: The Jetson TX2 NX contains one USB-SS port. The PORTSC offset and pin # are:
>
> USB_SS#1 is from USBSS (pins 161/163/166/168), offset = 0x430
>
> Refer to software release documentation for information on supported mapping configuration.
>
> Writing 0x10340 will change the internal state of XUSB. Therefore, it is not expected to read back the same value.
>
> If devmem2 commands result in a "bus error," try other versions or other register read/write tools

6. Launch the USB3.0 test application from the scope and press OK until it is waiting for the LFPS signals.
7. Connect the USB3.0 Host Test Fixture to the DUT (the application should be able to see the LFPS signals) and start compliance test.
8. Confirm DUT is in compliance mode by checking XUSB_XHCI_OP_PORTSC[8:5] = 0xA.

Placing Jetson TX2 NX in Loopback Mode

To run the RX electrical compliance test, the Jetson TX2 NX must be placed in loopback mode. To achieve this, disable runtime power management for USB Host Controller.

Linux for Tegra Image

1. Boot up the DUT (ensure the USB3.0 Host Test Fixture is not connected to the DUT).
2. Install the latest Linux for Tegra Image.
3. Run the following script to disable power management for USB Host Controller.

```
#!/bin/sh
for hub in $(ls -d /sys/bus/usb/devices/usb?); do
echo on > $hub/power/control
done
```

4. Connect the USB3.0 Host Test Fixture to the DUT and start compliance test.

Equipment Selection for RX Tolerance Tests

NVIDIA SuperSpeed USB PHY RX tolerance tests have been conducted with the Tektronix BERTScope, Agilent JBERT, and LeCroy PeRT3 platforms. During the testing process it was found that the SuperSpeed USB PHY passes with both Tektronix and Agilent equipment but not the LeCroy test setup.

The *Universal Serial Bus 3.0 Specification*, Revision 1.0 defines loopback mode to facilitate RX Jitter Tolerance testing. Entry to loopback mode is achieved by sending a specific sequence of patterns. Error rate tester sets the loopback bit in TS2 ordered sets while training the link for loopback entry sequence. Section 6.8.4.1 of the USB3.0 specification clearly states that during loopback the receiver processes the BERT ordered sets BRST, BDAT, and BERC. However, this sequence is not being followed by many testers. The fundamental assumption with Agilent and LeCroy testers is that loopback mode is immediately entered after TS2 handshake with loopback bit set. However, the XUSB design implemented in the Jetson TX2 NX looks for BRST ordered set to complete loopback in compliance with Section 6.8.4.1 of the USB3.0 specification.

Table 5.   Loopback Entry + Error Checking Sequences

Tektronix BERTScope	Agilent JBERT	LeCroy PeRT3
Polling.LFPS	Polling.LFPS	Polling.LFPS
TSEQ	TSEQ	TSEQ
TS1	TS1	TS1
TS2	TS2	TS2
BRST+CP0	COM	COM+D10.2
CP0 error checking	CP0 error checking	CP0 error checking

Different vendors use different sequences. The Jetson TX2 NX USB3.0 controller follows the Tektronix sequence for loopback entry and error checking. Tektronix BERTScope introduces BRST for jitter tolerance testing and we can successfully enter loopback without modifications to the sequence. Since the Agilent JBERT and LeCroy PeRT3 testers do not introduce BRST and we consequently fail to start loopback testing because loopback is not achieved.

This incompatibility does not affect USB3.0 functionality in any way.

It is possible to modify the Agilent JBERT sequence to introduce BRST, as shown in Table 6 by inserting a "pause" in the JBERT automation software after COM has been transmitted and manually running BRST sequence before completing the error checking sequence.

Table 6.   Modified JBERT Sequence

Agilent JBERT
Polling.LFPS
TSEQ
TS1
TS2
COM
BRST
CP0 error checking

The Jetson TX2 NX XUSB loopback sequence is incompatible with this pattern and it puts the Jetson TX2 NX into a bad state causing LeCroy PeRT3 to lose sync. It is not possible to transmit a modified sequence to put the Jetson TX2 NX USB3.0 controller back into loopback after the COM+D10.2 pattern because LeCroy PeRT3 is not able to re-sync. Therefore, it is currently not possible to test the Jetson TX2 NX SuperSpeed USB PHY receiver using LeCroy PeRT3.

The Jetson TX2 NX SuperSpeed USB PHY pass RX tolerance tests with both Tektronix and Agilent platforms. Therefore, NVIDIA recommends designers use Tektronix or Agilent (with modified sequence) equipment for their testing. The behavior described in this application note is due to a different interpretation of the USB3.0 specification and does not affect USB3.0 operational performance nor does it cause compliance failures. It only affects the sequence required for loopback entry.

Jetson TX NX PCIe Compliance Testing Reference

NVIDIA Jetson TX2 NX includes the Peripheral Component Interconnect Express (PCIe) interface. The implementation in Jetson TX2 NX supports both 2.5 G (PCIe Gen1) and 5.0 G (PCIe Gen2) transfer rates.

This chapter describes the test equipment, software, and setup required to run the PCIe Gen1 and Gen2 electrical compliance tests. The Jetson TX2 NX has been tested under worst-case scenarios and the hardware can adapt to the compliant devices and channel automatically. The hardware calibrates the termination impedance for both PCIe transmitter and receiver, adjusts the output amplitude, and the receiver fully adapts any internal parameter that is required. Additionally, it performs periodic equalization for the higher speed signals to compensate for temperature effect. Therefore, no tuning will be required if customer designs follow the routing guidelines published in our design guide.

The lane mappings for the configurations are internal to the PCIe root port controller. For the supported configurations, refer to the *Jetson TX2 NX Product Design Guide*.

Equipment

The components required to perform PCIe compliance testing include:
- ▶ Test Fixture
- ▶ Oscilloscope
- ▶ Probe
- ▶ Cables
- ▶ Termination Load/Adapter
- ▶ Software
  - PCISIG Clock Jitter Tool
  - SigTest 3.2.0 Software, or similar
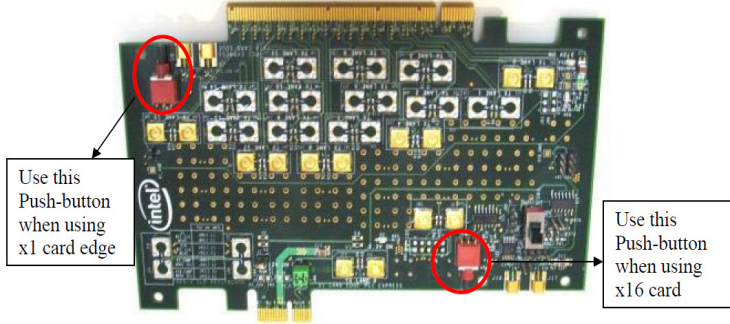
There are many tools currently available to help with compliance testing. The following sections list some of the equipment available. Items marked with an asterisk (*) indicate equipment that NVIDIA has used in its testing.

Test Fixtures

Test fixtures are used to connect the probes to the TX pins of the PCIe interface. Fixtures of different interface types are available and are recommended as opposed to adapters to convert the interface Type. Whichever fixture is selected, it must have SMP interconnects to avoid impedance mismatches due to discontinuities.

Table 7.   PCIe Test Fixtures Partial List

Product	Image and Description
PCIe Gen2 CLB v2 (for desktop CEM) See Note	Use this Push-button when using x1 card edge / Use this Push-button when using x16 card

Notes: CLB is Revision 2.0 or higher Compliance Board.

There are two different versions of CLB:

- x1/x16 which has x1 and x16 card edges for testing x1 and x16 motherboard slots
- x4/x8 which has x4 and x8 card edges for testing x4 and x8 motherboard slots

The Compliance Load Board (CLB) version(s) needed for testing a motherboard depend on the slot widths on the motherboard. All slots on the motherboard must be tested. Ordering information for the CLB can be found on PCISIG website at: http://pcisig.com/
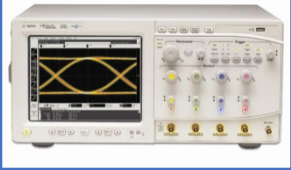
Oscilloscope

An oscilloscope is used to measure the signals.

PCIe Gen1

For PCIe Gen1, the PCIe specification requires that the oscilloscope have at least 6 GHz of bandwidth.

Table 8.   Instruments for PCIe Gen1 Partial List

Company	Product	Image and Description
Tektronix*	TDS6604B or better	
Agilent	DSO/DSA91304A or better	

PCIe Gen2

For PCIe Gen2, the PCIe specification requires that the oscilloscope have at least 12.5 GHz of bandwidth.

Table 9.   Instruments for PCIe Gen2 Partial List

Company	Product	Image and Description
Tektronix*	TDS6604B or better	
Agilent	DSO/DSA91304A or better	

Probes

Probes are used to connect the oscilloscope to the test fixture; oscilloscope probes must be a minimum of 8 GHz of bandwidth.

Table 10.   Probes Partial List

Company	Product	Image and Description
Tektronix*	1169A (Probe needs front attachment, based on test environment. Might require Agilent N5380A SMA adapter)	

Cables

Cables are used to measure signal quality.

Table 11.   Cables Partial List

Company	Product	Image and Description
Tektronix*	174-4944-xx Two pairs of matched SMA-SMA cables (skew <1ps)	
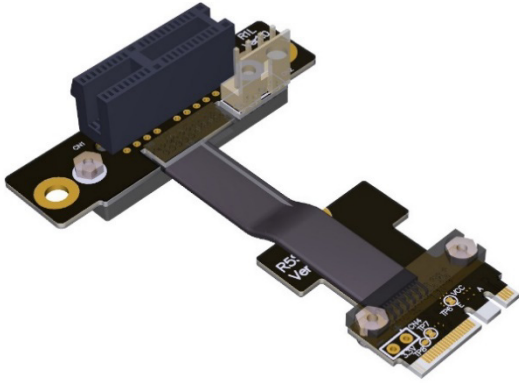
Company	Product	Image and Description
Pasternack*	P/N PE9514, Two pairs matched SMA-SMP adapters	
Tektronix*	Two pairs matched SMA-SMP cables	

Termination Load and Adapter

The following table is a list of termination load and adapters.

Table 12.   Termination Load and Adapter Partial List
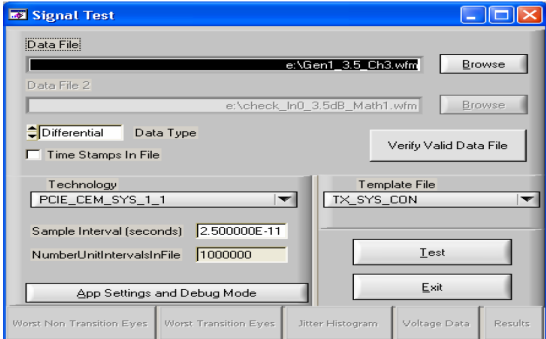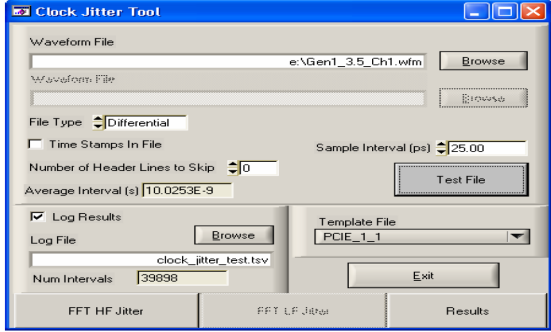
Product	Image and Description
50 Ohm Termination Load*	

Product	Image and Description
PCIe convert to M.2 Key E adapter	

Software

Use of official compliance test software is recommended, but not required. While manually measuring the signal might be just as effective, it must ultimately pass with the compliance software at the compliance house.

Table 13.   Recommended Test Software

Company	Product	Image and Description
PCISIG	SIGTEST 3.2.0	SIGTEST post processing analysis tool (version 3.2.0 or later): http://pcisig.com/developers/compliance-program
PCISIG	Clock Jitter Tool 1.3.0	Clock Jitter Tool (version 1.3.0 or later): http://pcisig.com/developers/compliance-program

Company	Product	Image and Description

PCIe Compliance Testing

PCISIG provides the compliance standards and test descriptions for system boards and add-in cards that comply with *PCI Express Card Electromechanical Specification* Revision 2.0. Customers should refer to the document for an overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure to perform the test.

PCI Express specification require devices to have a built-in mechanism for testing the electrical characteristics. Therefore, when the transmit lanes of the device are terminated with a 50-ohm load, the transmit lanes will automatically be forced into compliance mode.

To keep the PCIe controller enabled, the patch (rel-28_TegraX1_TegraX2.diff or rel-32_TegraX1_TegraX2.diff) attached to this application note should be applied.

1. The kernel source code can be downloaded from the L4T archive page (https://developer.nvidia.com/embedded/linux-tegra-archive). Choose the L4T version and download the code from the "Sources."

2. Apply the patch to the kernel source and follow the "Kernel customization" section from the developer guide (link can be found within the L4T archive) to build the kernel.

3. To update the kernel image, place the newly built image to the BSP directory (for example, Linux_for_Tegra/kernel/). To update loadable kernel modules, ensure the correct BSP path was specified (INSTALL_MOD_PATH=<top>/Linux_for_Tegra/rootfs/) when running Step 2.

4. To flash the board, follow the "Quick Start" section from the developer guide. A full flash should be completed to ensure all files gets updated.

To access the attached patch files, click the **Attachment** icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the file and use the Tool Bar options (**Open, Save**) to retrieve the files.

Testing with PCIe Devices

For compliance testing, CLB Version 2.0, which is the compliance load board, is required. If the DUT has an onboard PCIe device and hence does not have a PCIe slot or connectors, then the PCI device should be taken off from the board for CLB V2.0 to be hooked up.

Debugging

High speed I/O design is difficult to debug and will get harder as speeds increase. The following are a few common PCI Express issues.

If PCI Express Does Not Work

If PCI Express does not respond or no signals are being sent out, verify the following:

1. Check the applied power for expected value.
2. Check that clocks are on.
3. Check for chip reset de-assertion.
4. Check the power sequencing.

Figure 3.   Power Sequence Diagram
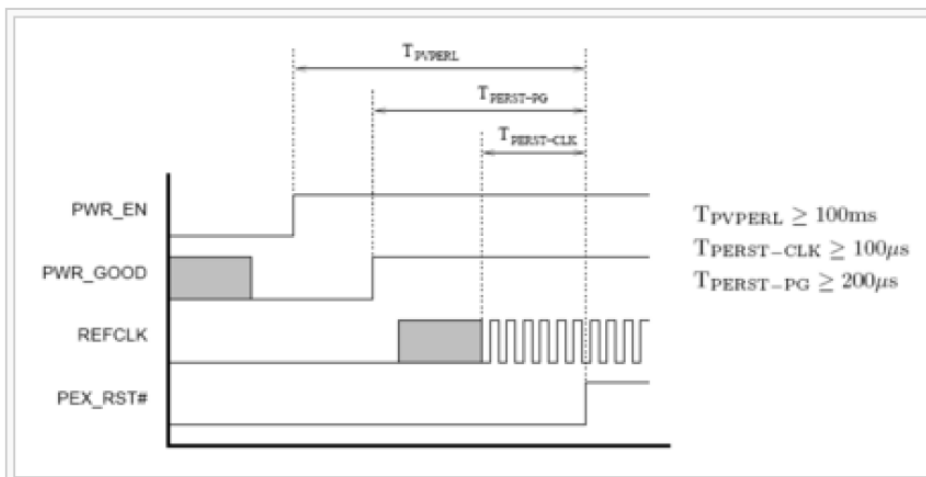
Device Fails at ASPM L0 or L1 Enabled

Connect device to a PCIe bus analyzer (For example, LeCroy Protocol Analyzer) to assist with the debug.

1. Configure analyzer to trigger on root repeatedly sending PM_Request_Ack DLLPs.
2. Capture the bus traffic at the time the bus failure occurs.

Jetson TX NX HDMI Compliance Testing

The Jetson TX2 NX uses HDMI™ technology. This chapter describes the registers and steps needed to tune the HDMI interface.

To meet HDMI compliance, tuning is required to adjust the TMDS signal such that the voltage swing is as close to 500 mV ± 100 mV, single-ended, or 1000 mV ± 200 mV differentially. This is to ensure the signal integrity is clean, meets the HDMI specifications, and the device is optimized for low power consumption.

> 💬 **Note**: Prior to any tuning, scope and probes must be calibrated. Refer to the documentation for your scope and probe for instructions on how to calibrate.

Figure 4.　　Source Eye Diagram CK-D2
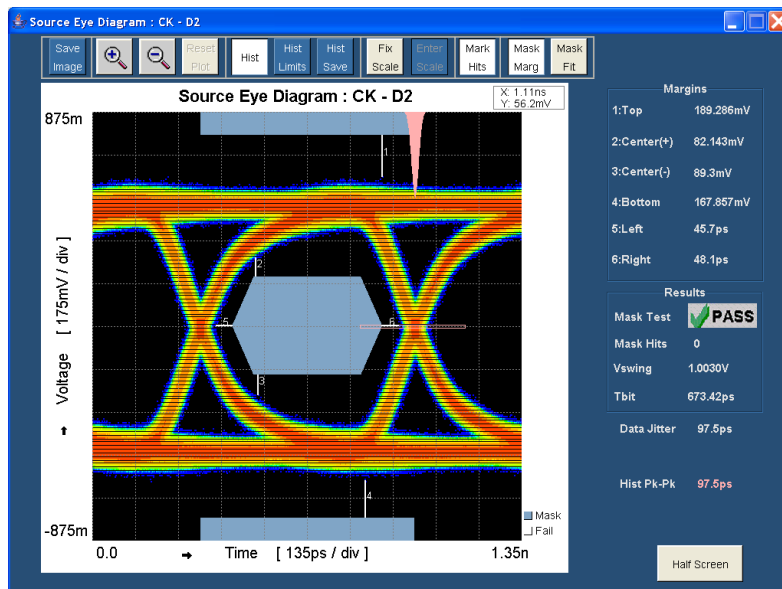
Abbreviations and Definitions

Table 14 lists the abbreviations that may be used throughout this chapter and their definitions.

Table 14.   Abbreviations and Definitions

Abbreviation	Definition
CTS	Compliance Test Specification
DUT	Device Under Test
EMI	Electromagnetic Interference
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
PVT	Process, Voltage, and Temperature
RF	Radio Frequency
Sink	Any type of receiver, such as a display or panel
SOR	Serial Output Resource – Module naming referring to the HDMI block
Source	Any type of transmitter, such as Tegra
TMDS	Transition-Minimized Differential Signaling

Setup

This section provides the setup and required equipment for HDMI tuning on Jetson TX2 NX.

Required Equipment

There are many tools currently available to perform the HDMI tuning. These are the required components:

- ▶ Test fixture
- ▶ Oscilloscope
- ▶ Software
  - • HDMI compliance software
  - • Tools to access register space in Tegra
- ▶ DC power supply

The following subsections list some of the acceptable equipment that may be used.

> **Note**: The items listed in the sections that follow are the tools NVIDIA used for its own validation and tuning. This chapter will refer to those tools specifically.
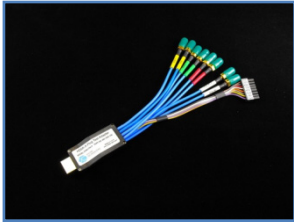
Test Fixture

Test fixtures are used to connect the probes to the output of the HDMI interface. The following example fixtures listed use the Type A interface for HDMI 1.4b compliance. Fixtures of different interface types are available and are recommended over using adapters to convert the interface type.

For HDMI 2.0 compliance, ensure that the test fixture can support the higher bitrate with minimal insertion loss.

The fixture selected must have SMA interconnects to avoid impedance mismatches due to discontinuities.

Table 15.   Partial List of Acceptable HDMI Test Fixtures Type A

Efficere	EFF-HDMI-TPA-P	
Agilent	N1080A	
Wilder Tech.	HDMI-TPA-P	

Oscilloscope
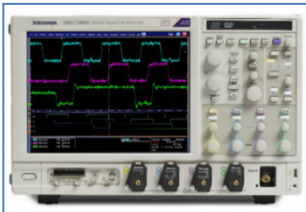
The oscilloscope is used to display and measure the signals. The HDMI 1.4 specification requires that the oscilloscope have at least 8 GHz of bandwidth and a sampling rate of at least 10 GS/s if the pixel clock is equal to or less than 165 MHz, or sampling rate of at least 20 GS/s if the pixel clock is greater than 165 MHz.

Table 16.   Partial List of Acceptable Oscilloscopes for HDMI 1.4 Tuning

Tektronix	TDS6804B or better	
Agilent	DSO80000B or better	

An oscilloscope with at least 16 GHz of bandwidth is recommended for HDMI 2.0.

Table 17.   Partial List of Acceptable Oscilloscopes for HDMI 2.0 Tuning

Tektronix	DPO/MSO 70000 series 16 GHz or better	
Agilent	Infiniium 90000 series 16 GHz or better	

Probes

Probes are used to connect the scope to the test fixture. The probes must have at least 8 GHz of bandwidth for HDMI 1.4b testing and at least 12 GHz of bandwidth for HDMI 2.0 testing.

At least 2 probes are required for tuning, however, 4 probes are ideal.

Untested lanes must be terminated appropriately. See the "DC Power Supply" section for details.

Table 18. Partial List of Acceptable Probes

Tektronix	P7313SMA	
Agilent	1169A Requires Agilent N5380A	
Agilent	N5380A Used with Agilent 1169A	

Power Supply

Any power supply that can supply a constant voltage of 3.3V is needed to terminate the HDMI signals. Refer to the probe's instruction manual on how to supply this termination voltage to the probes.

> 📝 **Note**: On Jetson TX2 NX, untested lanes must be terminated to 3.3V using 50 Ω terminators. Irrespective of the tools used, it is important to make sure that they are calibrated and meet industry standards to obtain accurate measurements.
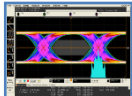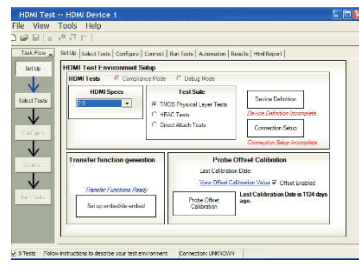
Software

This section details the software for the HDMI compliance testing.

Compliance Test Software

It is recommended to use the official compliance test software to ensure accurate results. Although manually measuring the signal may be just as effective, it must ultimately pass with the compliance software at the compliance house.

Table 19.   Partial List of Acceptable Test Software

	HDMI 1.4b Testing		HDMI 2.0 Testing	
Tektronix	TDSHT3 or later		TekExpress HDM or later	
Agilent	N5399A or later		N5399C or later	

Tegra Software Tools

Consult your software team or contact your NVIDIA representative for assistance with software tools to access the register space in Tegra.

Method for Tuning

Tuning is done by running the eye diagram tests on each of the data lanes while shmoo'ing the applicable registers. The objective is to keep the differential voltage swing as close to 1000 mV as possible, while providing the eye diagram enough margin to meet specifications.

Internal Termination

To effectively shmoo for the correct voltage swing, the drive strength can be estimated by calculating the parallel resistance to AVDD_HDMI/AVcc, assuming exact 50 ohms to 3.3V in the receiver. The equivalent resistance can be calculated based on the internal resistance settings. Then refer to the register description section for the current per drive strength tap to calculate the voltage swing.

With the equivalent termination and current per drive strength, the approximate voltage swing can be calculated. However, for higher speeds and routing differences, increased drive strength and pre-emphasis may be needed to overcome signal loss due to routing or EMI damping components.

On Jetson TX2 NX, the internal termination has an internal calibration mechanism which calibrates the internal termination to 50 Ω, depending on the external RSET value, silicon variation, and temperature variation.

To manually perform the calibration, use a binary search:

1. Set PAD_CAL_PD to 0.
    Use SOR_NV_PDISP_SOR_DP_PADCTL0_0 for SOR0 and
    SOR_NV_PDISP_SOR_DP_PADCTL0_1 for SOR1.

2. Start with the most significant bit by setting TMDS_TERMADJ to 0x8 (4'b1000).

3. Wait 100 uS and read COMPOUT.

4. If COMPOUT is 0x1, set the bit to 0. Else, keep the bit set to 1.

5. Move to the next significant bit and repeat until all 4 bits are determined.

6. Repeat this process at least 3 times, since the COMPOUT output is analog.

7. Set PAD_CAL_PD to 1.

Procedures

Calibrate the scope and probes before you begin. Refer to your scope and probe user manuals for details on how to calibrate.

DUT

This chapter does not cover setup of HDMI at the desired resolution. Work with your software team and NVIDIA representative to prepare the DUT for testing.

1. Disable Hot Plug Detect: The driver or OS may disable HDMI if it detects the panel being disconnected. To prevent this, choose one of the following 2 methods.

    a). Method 1: Disable the HPD interrupt via software by setting the HPD pin to TRISTATE.

    b). Method 2: Disconnect the HPD circuit from the HDMI connector. Refer to the DUT schematics: If this method is chosen, the circuit must be restored before performing the HDMI certification tests.

2. Configure the DUT to drive HDMI at the supported resolutions: 480p (27 MHz), 720p (74.25 MHz), 1080p (148.5 MHz), 2160p/30 (297 MHz), or 2160p/60 (590 MHz).

3. Attach the test fixture to the DUT.

4. Attach the probe-ends to the test fixture, and properly connect the termination voltage to the probes. Untested lanes must be properly terminated.

5. Attach the probes to the scope.

Oscilloscope

1. Ensure the probes are using the termination voltage of 3.3V.

2. Start the HDMI compliance software.

3. Setup the HDMI compliance software to take the eye diagram and configure the probes to the proper clock and data assignments.

4. Run the eye diagram test.

5. Record the voltage swing and margins (see Figure 5).

6. Refer to the "Registers" section and note the internal termination, drive strengths, and pre-emphasis settings.

7. Repeat for all data lanes, using different register settings, at all supported resolutions.

> **!** **Tips**:
> - When shmoo'ing drive strengths or pre-emphasis, keep the same value across each data lane. The HDMI pads for each of the data pairs and the clock are the same and should have very minor variation.
> - Since the clock does not have as many transitions, the settings can be weaker than the data lanes. This can save some power and lower possible noise or EMI.

Figure 5. Voltage Swing and Margins Results
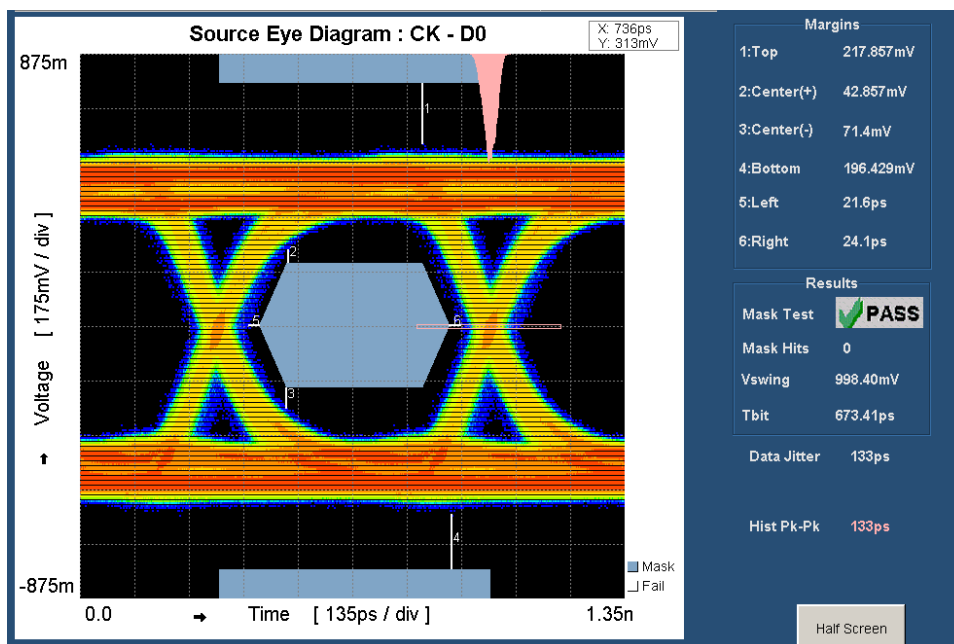
Objectives

While there is no margin specification, a good rule of thumb is to provide:

▶ At least 40 mV of margin above and below the eye mask

▶ Voltage swing of around 1000 mV

▶ Find settings for:

- 480p
- 720p
- 1080p
- 2160p/30
- 2160p/60

> **!** **Tips**:
> - Lower drive strength, IO peak current, and pre-emphasis settings will lower the power consumption.
> - The stronger the termination, more current is needed and therefore a higher power consumption.
> - Fast rising/falling edges will contribute to increased EMI.

Voltage Swing Target

This section targets a differential voltage swing of 1000 mV.

The target can be lowered to help reduce EMI and RF related issues.

> **!** **CAUTION**: If the user lowers the differential voltage swing target, the user assumes complete responsibility for issues or consequences arising as a result. In addition, the user must test random parts to ensure HDMI compliance with the new differential voltage settings.

Registers

The Serial Output Resource (SOR) module can be configured to output HDMI™ or VESA® DisplayPort™ (DP). Jetson TX2 NX has two instances of the SOR module and two sets of **HDMI_DP** pins. SOR0 controls the **HDMI_DP0** pins and SOR1 controls **HDMI_DP1**. To select which SOR to access, simply replace the trailing number with the SOR number. For example; **SOR_NV_PDISP_SOR_PLL1_0** for the first SOR and **SOR_NV_PDISP_SOR_PLL1_1** for the second SOR.

Table 20. HDMI_DP0 SOR0 Registers

Register Name	Bit Fields	Description	Notes
SOR_NV_PDISP_SOR_PLL1_0 (Address: 0x15540590)			
RESERVED	31:16	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TMDS_COMPOUT	15:15	Internal Termination Calibration Comparator Output	When calibrating the internal termination, this read-only register will output 0 if the termination is lower than 50Ω and 1 if the termination is higher.
RESERVED	14:14	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TMDS_TERMADJ	12:09	Internal Termination Resistance Control	Requires TMDS_TERM to be enabled.
TMDS_TERM	08:08	Internal Termination Enable	Enables internal termination
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
SOR_NV_PDISP_SOR_PLL3_0 (Address: 0x15540598)			
RESERVED	31:28	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
BG_VREF_LEVEL	27:24	Bandgap Voltage Level	Changes the reference voltage used to generate the current for the pads. Higher settings equate to higher current draw per tap for DRIVE_CURRENT and PREEMPHASIS.
RESERVED	23:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_0 (Address: 0x15540138)			
LANE3_DP_LANE3	31:24	Drive Strength Controls for the Clock Lane for HDMI and Lane 3 for DP/eDP	Each tap increases the drive strength by 0.400mA, with a base of 0.000mA.
LANE2_DP_LANE0	23:16	Drive Strength Controls for Lane 2 for HDMI and Lane 0 for DP/eDP	000.0000 → 0.000mA 000.0001 → 0.400mA ...
LANE1_DP_LANE1	15:08	Drive Strength Controls for Lane 1 for HDMI and Lane 1 for DP/eDP	011.0000 → 19.200mA (starting to borrow from pre-emphasis drivers)
LANE0_DP_LANE2	07:00	Drive Strength Controls for Lane 0 for HDMI and Lane 2 for DP/eDP	100.0111 → 28.200mA (max) 100.1000 → 25.400mA

Register Name	Bit Fields	Description	Notes
SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_0 (Address: 0x15540148)			
LANE3_DP_LANE3	31:24	Pre-Emphasis Controls for the Clock Lane for HDMI and Lane 3 for DP/eDP	Pre-emphasis controls take lower precedence than drive strength and may not have any noticeable effect at higher drive strengths. Refer to the TRM for more detailed information.
LANE2_DP_LANE0	23:16	Pre-Emphasis Controls for Lane 2 for HDMI and Lane 0 for DP/eDP	
LANE1_DP_LANE1	15:08	Pre-Emphasis Controls for Lane 1 for HDMI and Lane 1 for DP/eDP	
LANE0_DP_LANE2	07:00	Pre-Emphasis Controls for Lane 0 for HDMI and Lane 2 for DP/eDP	
SOR_NV_PDISP_SOR_DP_PADCTL0_0 (Address: 0x155405A0)			
RESERVED	31:24	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
PAD_CAL_PD	23:23	Pad Calibration Power Down	Set to 0 to enable calibration, 1 to disable
TX_PU	22:22	Transmitter pull-up resistors.	Enables the pull-ups for the current sources.
RESERVED	21:16	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TX_PU_VALUE	15:08	TX pull-up current source drive	Provides additional current for the current drivers. Can help improve the transition edge speeds and overall voltage swings.
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.

Table 21.   HDMI_DP1 SOR1 Registers

Register Name	Bit Fields	Description	Notes
SOR_NV_PDISP_SOR_PLL1_1 (Address: 0x15580590)			
RESERVED	31:16	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TMDS_COMPOUT	15:15	Internal Termination Calibration Comparator Output	When calibrating the internal termination, this read-only register will output 0 if the termination is lower than 50 Ω and 1 if the termination is higher.
RESERVED	14:14	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TMDS_TERMADJ	12:09	Internal Termination Resistance Control	Requires TMDS_TERM to be enabled.
TMDS_TERM	08:08	Internal Termination Enable	Used to enable internal termination
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
SOR_NV_PDISP_SOR_PLL3_1 (Address: 0x15580598)			
RESERVED	31:28	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
BG_VREF_LEVEL	27:24	Bandgap Voltage Level	Changes the reference voltage used to generate the current for the pads. Higher settings equate to higher current draw per tap for DRIVE_CURRENT and PREEMPHASIS.
RESERVED	23:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
SOR_NV_PDISP_SOR_LANE_DRIVE_CURRENT0_1 (Address: 0x15580138)			
LANE3_DP_LANE3	31:24	Drive Strength Controls for the Clock Lane for HDMI and Lane 3 for DP/eDP	Each tap increases the drive strength by 0.400mA, with a base of 0.000mA.
LANE2_DP_LANE0	23:16	Drive Strength Controls for Lane 2 for HDMI and Lane 0 for DP/eDP	000.0000 → 0.000mA 000.0001 → 0.400mA ...
LANE1_DP_LANE1	15:08	Drive Strength Controls for Lane 1 for HDMI and Lane 1 for DP/eDP	011.0000 → 19.200mA (starting to borrow from pre-emphasis drivers)
LANE0_DP_LANE2	07:00	Drive Strength Controls for Lane 0 for HDMI and Lane 2 for DP/eDP	100.0111 → 28.200mA (max) 100.1000 → 25.400mA

Register Name	Bit Fields	Description	Notes
SOR_NV_PDISP_SOR_LANE_PREEMPHASIS0_1 (Address: 0x15580148)			
LANE3_DP_LANE3	31:24	Pre-Emphasis Controls for the Clock Lane for HDMI and Lane 3 for DP/eDP	Pre-emphasis controls take lower precedence than drive strength and may not have any noticeable effect at higher drive strengths. Refer to the TRM for more detailed information.
LANE2_DP_LANE0	23:16	Pre-Emphasis Controls for Lane 2 for HDMI and Lane 0 for DP/eDP	
LANE1_DP_LANE1	15:08	Pre-Emphasis Controls for Lane 1 for HDMI and Lane 1 for DP/eDP	
LANE0_DP_LANE2	07:00	Pre-Emphasis Controls for Lane 0 for HDMI and Lane 2 for DP/eDP	
SOR_NV_PDISP_SOR_DP_PADCTL0_1 (Address: 0x155805A0)			
RESERVED	31:24	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
PAD_CAL_PD	23:23	Pad Calibration Power Down	Set to 0 to enable calibration, 1 to disable
TX_PU	22:22	Transmitter pull-up resistors.	Enables the pull-ups for the current sources.
RESERVED	21:16	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.
TX_PU_VALUE	15:08	TX pull-up current source drive	Provides additional current for the current drivers. Can help improve the transition edge speeds and overall voltage swings.
RESERVED	07:00	RESERVED REGISTERS	Register field is RESERVED. Do not modify; preserve existing value.

Final Check

After tuning is completed, the settings should be sanity-checked to make sure they have not violated any other parts of the HDMI specifications and that there is a comfortable amount of margin.

The DUT should go through the battery of electrical tests outlined in the *HDMI Compliance Test Specifications* (CTS) document to ensure that the DUT passes HDMI certification.

If there are any failures, the settings must be tuned again until there is a passing result.

> **Note**: Higher power consumption is expected if the new settings are stronger than the default settings. It may be due to, but not limited to, longer traces, EMI chokes on the signal paths, or signal integrity issues.

Updating the Software

After the tuned settings have been verified, they need to be updated into the OS or the driver. Contact the appropriate software team, or your NVIDIA representative with the new tuned settings.

▶ The 480p settings apply to pixel clock resolutions ⩽ 54 MHz
▶ The 720p settings apply to pixel clock resolutions between > 54 MHz to ⩽ 111 MHz
▶ The 1080p settings apply to pixel clock resolutions between > 111 MHz to ⩽ 223 MHz
▶ The 2160p/30 settings apply to pixel clock resolutions between > 223 MHz to ⩽ 297 MHz
▶ The 2160p/60 settings apply to all HDMI 2.0 resolutions

> **Note**: Ranges can be adjusted according to design and use cases. More ranges can also be defined if proper tuning and software implementation is performed.

Final Steps

After the settings have been updated in the driver, you must verify that the tuned settings are being applied for each of the target resolutions.

A visual check-out is recommended as well. Connect the DUT to an HDMI or DVI panel and visually verify that there is no corruption at any of the supported HDMI resolutions.

Jetson TX2 NX Ethernet Compliance Test Guide

This chapter serves as the high-level guide to compliance testing of the 1000Base-T interface in NVIDIA Jetson TX2 NX. The Jetson TX2 NX has been tested for specification compliance; therefore, no tuning will be required if customer designs follow the routing guidelines published in our design guides.

Compliance Testing

The IEEE Standard for Ethernet defined by IEEE802.3ab provides the compliance criteria and test descriptions for 1000Base-T. Customers should refer to the document for a high-level overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure to perform the test.

Tools

Mdio-tool is a generic tool which can be used to access the PHY registers from the Linux command line. It can be downloaded and compiled from the following location: https://github.com/PieVo/mdio-tool

> 📝 **Note**: The original makefile is for cross-compilation, therefore it can be built directly on the device through the command "gcc -o mdio-tool mdio-tool.c"

Placing Jetson TX2 NX in Compliance Mode

The Jetson TX2 NX integrates a Realtek RTL8211F(I) Gigabit Ethernet PHY. Therefore, to perform compliance testing on the Jetson TX2 NX, customers will need to contact Realtek to obtain documentation on how to access the internal registers.

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