Jetson Orin NX Series and Jetson Orin Nano Series Tuning and Compliance Guide

Application Note

Document History

DA-11267-001_v1.0

Version	Date	Description of Change
0.5	January 20, 2023	Preliminary release
0.7	March 8, 2023	Updated PCIe power down disable patch attachment.
0.9	April 5, 2023	> Updated Section: Patch Attachments with information regarding PCIe power down disable and spread spectrum disable patches and added instructions. > Added Section: Ethernet Compliance Test Guide.
1.0	October 4, 2023	> Added sub-section: Slew Rate for **HDMI** under Section: Method for Tuning. and corresponding registers in Table 15:.Orin SOR Registers for HDMI. > Updated table captions for Table 15 and Table 19. > Updated binary representation for the register: NV_PDISP_SOR_DP_PADCTL0_0: Address 0x1380c130 in Table 19: Orin SOR Registers for DisplayPort.

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Overview

This application note is the tuning and compliance guide for NVIDIA® Jetson™ Orin NX series and Jetson Orin Nano™ series modules. This application note details the following:

- USB tuning and compliance testing
- PCIe compliance testing
- HDMI™ tuning
- VESA® DisplayPort® and embedded DisplayPort tuning
- Ethernet compliance testing

Note: All occurrences of “Orin module” refers to Jetson Orin NX series and Jetson Orin Nano series modules.

USB 2.0 Tuning Guide

This chapter describes the steps and lists the registers needed to tune the USB 2.0 high-speed eye diagram for the Orin modules. The USB Implementers Forum (USB IF) provides complete test specifications and instructions on their website for high-speed host and device mode testing.

NVIDIA typically uses Tektronix oscilloscopes for USB characterizations. The test procedures for Tektronix oscilloscopes are available from the USB-IF website.

Customers may use oscilloscopes from other vendors to perform USB characterization.

Required Equipment

The following equipment is required:

- Tektronix TDS694C or faster digital sampling oscilloscope.
- Tektronix P6247 or P6248 or equivalent differential probe.
- High-speed USB electrical test fixture.
- Oscilloscope USB test software.
- Software tool to access register and memory space on the Orin module or to build a special image to force the enable of the USB test mode.

Host Mode Testing Registers

Table 1 lists the USB 2.0 registers that must be toggled to force Test J, Test K, Test SE0 NAK, and Test packet on the respective USB ports.

Table 1. Host Mode Test Registers

Description	Register Name and Setting
Normal operations	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0000b
Test J	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0001b
Test K	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0010b
Test SE0 NAK	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0011b
Test packet	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0100b
Force enable	T_XUSB_XHCI_OP_PORTPMSCHS_x[31:28] = 0101b

The xUSB USB 2.0 port register addresses are as follows:

- Port 0: 0x03610464: T_XUSB_XHCI_OP_PORTPMSCHS_4
- Port 1: 0x03610474: T_XUSB_XHCI_OP_PORTPMSCHS_5
- Port 2: 0x03610484: T_XUSB_XHCI_OP_PORTPMSCHS_6

Note: NVIDIA uses the equipment listed for this guide. Contact the vendor for compliance Oscilloscope and software.

Test Mode Programming Sequence

The programming sequence for enabling USB 2.0 test mode is as follows:

1. Connect any USB device (see “Note”) to the port. This will prevent the controller from entering power down mode.

Note: The phrase “any USB device” refers to any real device, such as HS uDISK or LS mouse

2. Disable the auto suspend for the controllers. For example, the following command under Linux Kernel.

Note: These operations require root privileges.

```
Echo on > /sys/bus/usb/devices/usb1/power/control
```

3. Set Port Power (PP) to Disabled state by setting T_XUSB_XHCI_OP_PORTSC[9] = 0

   Port 0: 0x03610460: T_XUSB_XHCI_OP_PORTSC_4

   Port 1: 0x03610470: T_XUSB_XHCI_OP_PORTSC_5

   Port 2: 0x03610480: T_XUSB_XHCI_OP_PORTSC_6

4. Set RS (Run/Stop) bit in the T_XUSB_XHCI_OP_USBCMD_0[0] = 0.

   0x03610020: T_XUSB_XHCI_OP_USBCMD_0
5. Wait for the HCHalted (HCH) bit in the T_XUSB_XHCI_OP_USBSTS_0[0] = 1.

   0x03610024: T_XUSB_XHCI_OP_USBSTS_0
6. Set the xUSB Port Test Control registers in PORTPMSCHS register. See “Host Mode Testing Registers” section.

> **Note:** Per USB 2.0 specification, only a single downstream facing port can be in test_mode at a given time.

7. Disable Pad PD (power down) by clearing the T_XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0[26] = 0.

   Port 0: 0x03520088: T_XUSB_PADCTL_USB2_OTG_PAD0_CTL_0_0

   Port 1: 0x035200C8: T_XUSB_PADCTL_USB2_OTG_PAD1_CTL_0_0

   Port 2: 0x03520108: T_XUSB_PADCTL_USB2_OTG_PAD2_CTL_0_0
8. Plug in the test fixture to start the USB 2.0 eye diagram test.

USB 2.0 Eye Diagram Registers

Table 2 lists the NVIDIA Orin™ USB registers that are needed to tune the USB 2.0 eye diagram. See “Tuning Procedure and Registers” section on how to use these registers during characterization.

Table 2. NVIDIA Orin USB Registers

Register Name	Bit Field	Description
XUSB_PADCTL_USB2_OTG_PAD0_CTL_0_0 (Address 0x03520088) for Port 0 XUSB_PADCTL_USB2_OTG_PAD1_CTL_0_0 (Address 0x035200C8) for Port 1 XUSB_PADCTL_USB2_OTG_PAD2_CTL_0_0 (Address 0x03520108) for Port 2		
HS_SLEW (See Note 1)	8:6	HSSLEW (high-speed slew rate control)
HS_CURR_LEVEL (See Note 2)	5:0	Setup (high-speed drive strength control)
XUSB_PADCTL_USB2_OTG_PAD0_CTL_1_0 (Address 0x0352008C) for Port 0 XUSB_PADCTL_USB2_OTG_PAD1_CTL_1_0 (Address 0x035200CC) for Port 1 XUSB_PADCTL_USB2_OTG_PAD2_CTL_1_0 (Address 0x0352010C) for Port 2		
RPD_CTRL	30:26	RPD_CTRL (15K host pull-down)
TERM_RANGE_ADJ	6:3	ATERM (high-speed termination control)
XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0 (Address 0x03520284)		
HS_SQUELCH_LEVEL	2:0	HSSQUELCH (squelch level control for device RX testing)

Register Name	Bit Field	Description
XUSB_PADCTL_USB2_OTG_PAD0_CTL_3_0 (Address 0x03520094) for Port 0 XUSB_PADCTL_USB2_OTG_PAD1_CTL_3_0 (Address 0x035200D4) for Port 1 XUSB_PADCTL_USB2_OTG_PAD2_CTL_3_0 (Address 0x03520114) for Port 2		
HS_RXEQ (See Note 3)	7:6	HS_RXEQ (device RX testing)
HS_TXEQ (See Note 3)	2:1	HS_TXEQ (device TX testing)

Notes:

1. HS_SLEW where 0'b000 = slowest and 0'b111 = fastest.
2. HS_CURR_LEVEL where 0'b000000 = highest current level and 0'b111111 = lowest current level.
3. If system has inner cable, consult with AE for recommendations and perform certificate and functional test verification.

Table 3. TXEQ and RXEQ Pre-Emphasis

HS_TXEQ[1:0]	AC Gain	HS_RXEQ[1:0]	SQ Level
00	+0 dB (default)	00	-0 dB (default)
01	+1.3 dB	01	-1.2 dB
10	+2.5 dB	10	-2.0 dB
11	+3.5 dB	11	-3.5 dB

Tuning Procedure and Registers

During production, each Orin SoC is calibrated based on the silicon process, the corresponding USB drive strength (HS_CURR_LEVEL), HS termination (TERM_RANGE_ADJ), and a 15K host pull-down (RPD_CTL). As a result, fuses are burnt on each chip.

Table 4 lists the breakdown for the USB_CALIB and USB_CALIB_EXT fuses. Reading from the respective addresses will provide the default drive strength, HS termination, and 15K host pull-down value.

Table 4. USB_CALIB and USB_CALIB_EXT Fuses

Register Name	Bit Field	Description
USB_CALIB fuse (Address 0x038101F0)		
USB_CALIB	22:17	Drive strength for USB Port 2
USB_CALIB	16:11	Drive strength for USB Port 1
USB_CALIB	10:7	HS termination for USB Port 0
USB_CALIB	5:0	Drive strength for USB Port 0
USB_CALIB_EXT fuse (Address 0x03810350)		
USB_CALIB_EXT	12:9	HS termination for USB Port 2
USB_CALIB_EXT	8:5	HS termination for USB Port 1

Register Name	Bit Field	Description
USB_CALIB_EXT	4:0	USB pad 15k host pull-down for all ports

During the characterization stage, adjusting the HS_CURR_LEVEL value by modifying the USB register listed in Table 2 directly should be enough to fulfill compliance requirements. It is possible to try to increase termination as a last resort.

Note: Although it is possible to try to increase termination as a last resort, NVIDIA does not recommend adjusting termination values. NVIDIA cautions that if the TERM_RANGE_ADJ is adjusted, it may result in an impedance mismatch on the board and further attention might be needed.

Once the characterization stage has completed, if modification to HS_CURR_LEVEL is necessary, it must be done as an offset to the default fused value to account for silicon process differences.

Caution: Do not apply a global overwrite HS_CURR_LEVEL value for all silicon. Software should read the fuse USB drive strength and add an offset to it.

All other settings can be modified directly:

- To change high-speed slew rate, write directly to: XUSB_PADCTL_USB2_OTG_PADx_CTL_0_0 bits 8:6
- To change receive squelch level, write directly to: XUSB_PADCTL_USB2_BIAS_PAD_CTL_0_0 bits 2:0
- To compensate for long cable loss, use the XUSB_PADCTL_USB2_OTG_PADx_CTL_3_0 HS_TXEQ/HS_RXEQ bits directly.

HS_CURR_LEVEL Offset Adjustment Procedure

If the default values are not suitable to the customer design, adjust the HS_CURR_LEVEL register to pass the USB HS eye diagram.

Follow this procedure:

1. Adjust the HS_CURR_LEVEL register as described in the “Tuning Procedure and Registers” section to pass the USB HS eye diagram.
2. Obtain default value; read USB_CALIB fuse (Address 0x038201F0).

   USB_CALIB[5:0] USB pad HS_CURR_LEVEL[5:0] for Port 0

   USB_CALIB[16:11] USB pad HS_CURR_LEVEL[5:0] for Port 1

   USB_CALIB[22:17] USB pad HS_CURR_LEVEL[5:0] for Port 2
3. Calculate the offset from fused HS_CURR_LEVEL value and desired value from Step 1.
   a. For example, if default value is 0x20 and desired value is 0x1C, then offset = -4
   b. For example, if default value is 0x10 and desired value is 0x14, then offset = +4

Note: Maximum allowable offset: ±6 steps.

4. Provide the “tuned offset value” to software team so they can add the offset value when initializing the registers in Table 2.

Software Verification

NVIDIA strongly recommends a functional check. Connect the DUT to USB hosts and devices to perform a functional check.

To check if software has implemented the tuned offset correctly, load new software with offset included into another DUT and make sure that:

HS_CURR_LEVEL = USB_CALIB fuse + tuned offset steps.

USB 3.2 Compliance Test Guide

This chapter provides high-level guidance for compliance testing of the USB 3.2 PHY. It has a performance of up to Gen1 (5 Gb/s) and Gen2 (10 Gb/s) in host mode on the Orin module. The Orin module has been tested for specification compliance and has passed under worst-case scenarios. NVIDIA expects that no tuning will be required if customers follow the routing guidelines published in the relevant design guides.

Compliance Testing

The compliance criteria and test descriptions for USB 3.2 devices, hubs, and host controllers are based on the specification, *Electrical Compliance Test Specification SuperSpeed Universal Serial Bus Rev 1.0*.

The *Electrical Compliance Test Specification Enhanced SuperSpeed Universal Serial Bus Rev 1.0a* also provides the compliance criteria and test descriptions for SuperSpeed Plus USB devices, hubs, and host controllers that conform to the specification, *Universal Serial Bus 3.1 Specification, Rev 1.0*.

NVIDIA recommends that customer refer to the test specification documents mentioned for a high-level overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedures on how to perform the tests.

ⓘ	**Caution:** When the Orin module is in USB RCM mode, it may not be in compliance with the latest USB 3.2 specification.

USB 3.2 TX and RX Compliance Tests

To run the USB 3.2 TX electrical compliance test, the Orin module USB 3.2 controller must be put in compliance mode.

To run the RX electrical JTOL test, the Orin module must be trained to be in loop-back mode.

Putting the Orin Module USB 3.2 Controller in Compliance Mode

For Gen1 (5 Gb/p) TX electrical tests refer to sections TD.1.1, TD.1.3, and TD.1.4. For Gen2 (10 Gb/s) TX electrical tests, refer to sections: TD 1.4, TD 1.5, and TD1.7. These sections can be found in the *Electrical Compliance Test Specification SuperSpeed Universal Serial Bus Specification* at the following link: https://www.usb.org/document-library/electrical-compliance-test-specification-superspeed-usb-10-gbps-rev-10

Perform the following steps to place the device under test (DUT) into compliance mode:

1. Boot up the DUT. Ensure the USB 3.2 (Gen1 or Gen2) host test fixture is not connected to the DUT.
2. Install the latest OS (Linux, for example) image for the Orin module.
3. Install the devmem2 tool (for the Linux installed in Step 2, for example) by running the following command.
   ```
   $ sudo apt-get install devmem2
   ```
4. Launch the USB 3.2 Compliance Test Software on the scope.
5. Disable the auto suspend for the controllers:
   ```
   $ echo on > /sys/bus/usb/devices/usb1/power/control
   $ echo on > /sys/bus/usb/devices/usb2/power/control
   ```
6. Enter compliance test mode.
   ```
   $ ./devmem2 0x03610420 w 0x10340
   $ ./devmem2 0x03610430 w 0x10340
   $ ./devmem2 0x03610440 w 0x10340
   ```

Plug in the USB 3.2 host test fixture to DUT. The other end of fixture should be connected to a scope such that DUT TX± with 50 ohm termination on the scope.

For connection details refer to the “Transmitter Test Topologies” section in *USB 3.0 Electrical Test Fixture Topologies*, at the following link: https://www.usb.org/document-library/usb-31-electrical-test-fixture-topology

7. Use ./devmem2 0x3610420 (that is, for L0) command to read back the LTSSM state.

Notes: The Orin module contains three USB 3.2 ports.

The PORTSC offset and pin # are:

- HS_UPHY0_L0_TX/RX (pins F13/E13/B15/B16), offset = 0x420
- HS_UPHY0_L1_TX/RX (pins E12/D12/A14/A15), offset = 0x430
- HS_UPHY0_L2_TX/RX (pins F11/E11/B13/B12), offset = 0x440

Writing 0x10340 will change the internal state of XUSB. Therefore, it is not expected to read back the same value. However, Bits[8:5] should be set to 0xA for compliance test mode, otherwise repeat Step 1 through Step 7.

8. Connect RX± to external Ping.LFPS (20 MHz frequency; two periods) signal generator.

9. Sending a Ping.LFPS to the RX port of the DUT in compliance state will cause the compliance pattern to transition to the next one. Contact generator vendor for support to provide required number of Ping.LFPS until controller pumps out the required compliance pattern.
10. Based on compliance pattern (CP) requirement for the current test, repeat Step 9 to pump out required CP pattern.
11. Let the test complete.

Putting the Orin Module USB 3.2 Controller in Loop-Back Mode

To run the RX electrical JTOL test, the Orin module must be trained to be in the loop-back mode.

For Gen1 (5 Gb/s) electrical tests, refer to sections: TD 1.2, TD.1.8, TD.1.9 (for Type-C). For Gen2 (10 Gb/p) electrical tests, refer to sections: TD.1.2 and TD.1.10 in the *Electrical Compliance Test Specification SuperSpeed Universal Serial Bus Rev 1.0a*, at the following link: https://www.usb.org/document-library/electrical-compliance-test-specification-superspeed-usb-10-gbps-rev-10

Perform the following steps to put the DUT into loop-back mode:

1. Boot up the DUT. Make sure that the USB 3.2 host test fixture is not connected to the DUT.
2. Install the latest Linux image for Orin module.
3. Run the following script to disable power management for USB host controller.

```
#!/bin/sh
for hub in $(ls -d /sys/bus/usb/devices/usb?); do
echo on > $hub/power/control
done
```

4. For Gen 1x1 Configure BERT to pump out the loop-back training sequence, refer to Step 5 through Step 11 in Section “TD.1.8 Receiver Jitter Tolerance Test at GT/s” or “TD.1.9 Receiver Jitter Tolerance Test at GT/s (Type-C)” of the following specification: https://usb.org/sites/default/files/SuperSpeedPHYComplianceTest_Spec1_0a.pdf

   For Gen 2x1 upon detecting DUT Power On, refer to Step 14 through Step 18 in Section “TD.1.10 Receiver Jitter Tolerance Test at 10 GT/s” of the following specification: https://usb.org/sites/default/files/SuperSpeedPHYComplianceTest_Spec1_0a.pdf
5. Connect the USB 3.2 host test fixture to the DUT. For fixture topologies and connections for Gen1 and Gen2 RX testing, refer to the following: https://www.usb.org/document-library/usb-31-electrical-test-fixture-topology
6. Start JTOL test after the controller is in loop-back or repeat Step 1 through Step 5.
7. Let the test complete.

PCIe Compliance Testing Reference

Orin modules include several high-speed UPHY interfaces supporting protocols such as USB-3 and PCIe. Interface lanes can flexibly be mapped to PADs to form a mix of different protocols.

The Orin module supports several PCIe controllers. The controllers can be assigned to multiple UPHY lanes in two different domains (UPHY0 and UPHY2), in a mix with other controllers such as USB 3.2. Refer to the following documents for details:

- *Jetson Orin NX Series and Jetson Orin Nano Series Data Sheet*
- *Jetson Orin NX Series and Jetson Orin Nano Series Product Design Guide*
- *Orin Technical Reference Manual (TRM)*

The base requirement for all designs is to adhere to the *Jetson Orin NX Series and Jetson Orin Nano Series Product Design Guide* layout guidelines. PCIe shall pass all physical layer (PHY) specifications and conformance with no change in production (PROD) register settings. Changing the PROD settings is not recommended.

> **Caution:** Compliance testing and characterization as described in this application note covers PCIe Gen1 to Gen3 only.

The Tx test procedures described in this application note are not recommended for Gen4 and up, since they introduce higher amount of noise for measurements greater than Gen3 specifications. For higher speeds, functional testing and in-circuit test methods may be used. Such as Eye Opening Monitor (EOM)–an NVIDIA built-in UPHY facility, or PCIe “Lane Margining”–a mandatory support for devices with 16 GT/s or higher.

References

The following are PCIe specifications and NVIDIA documents references for PCIe compliance testing.

- PCISIG specifications:
  - *PCI Express Architecture PHY Test Specification 3.0* (Gen1, Gen2, and Gen3)
  - *PCI Express Architecture PHY Test Specification 4.0* (Gen1, Gen2, Gen3, and Gen4)

- NVIDIA document:
  - *Jetson Orin NX Series and Orin Nano Series Product Design Guide*

Patch Attachments

The following two files are attached to this application note:

- 319ad28_ok.diff: This file is the patch for disabling power down. The patch should be applied to the L4T kernel source. Follow the kernel customization section in developer guide to build and apply new kernel image.
- 0001-disabling-the-spread-Spectrum.patch: This file is the patch for disabling the spread Spectrum. Although it is a dts file patch, it is for the bpmp-dtb binary. End users need to disassemble the bpmp dtb (binary file), apply the patch, and then re-compile to dtb (binary file) with the steps below:
  - dtc -O dts -o bpmp.dtb.dts -I dtb <bpmp-dtb-file>.dtb
  - Apply the the patch “0001-disabling-the-spread-Spectrum.patch”
  - dtc -O dtb -o <bpmp-dtb-file>.dtb -I dts bpmp.dtb.dts

Note: The <bpmp-dtb-file>.dtb here depends on different platforms. Jetson Orin AGX, Orin NX, and Orin Nano may use different files.

To access the files, click the **Attachment** icon on the left-hand toolbar on this PDF (using Adobe Acrobat Reader or Adobe Acrobat). Select the files and use the Tool Bar options (**Open, Save**) to retrieve the files.

Electrical Characterization

This section details the electrical characterization for the PCIe compliance testing.

Prerequisites

Note the following prerequisites for electrical characterization.

- For a given design, boot the design using the OS to make sure all register settings (in particular, pad register settings) are in line with production environment.
- Make sure only the up-to-date modes supported by the Orin module for this interface are used. Refer to the *Jetson Orin NX Series and Orin Nano Series Product Design Guide*.
- Note that this application note only deals with chip-down. This means that characterization is performed for devices soldered down to the PCB. In case interfaces are realized through PCIe slots or connectors, a similar but different approach may be needed. This application note will highlight some but not all aspects

of characterization DUT setup where needed to avoid pitfalls. For all other information, refer to PCISIG specifications.

De-Embedding or Device Removal

Since this application note covers characterization for chip-down PCIe designs, the characterization procedure must include handling a chip-down environment. Removing the device is the standard way of characterizing chip-down PCIe connectivity. For PCIe transmit characterization, it is required to remove the connected device, while for PCIe device characterization it is required to remove the Orin module. Solder pads must be connected by proper interconnects (solder tips for probes or breakout boards) to the scope.

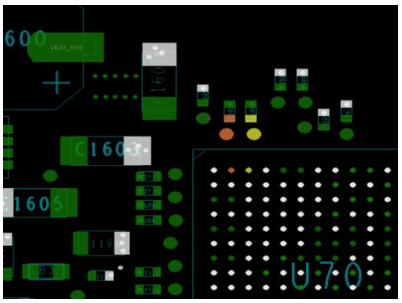
Note that when the Orin module supplies REFCLK to a device and when device is tested with the Orin module removed, REFCLK must be injected and supplied to the device. For more REFCLK specifics, see “REFCLK Measurement and Characterization” section.

The following figure shows part of an Orin module reference design.

Note the following:

- Device is removed to probe at the pins.
- In the example, the Orin module sourced REFCLK. It shall be injected from external source.

Figure 1. Device Removed from PCB for Characterization Example



Mid-Bus Probing

Note that mid-bus probing is not used by NVIDIA for characterization. Customers may use access points for probes that may be Rx or Tx coupling caps. Proper access to traces at coupling caps with the least possible distortion is required. Mid-bus probing is a less intrusive form of de-embedding. In turn, it requires S-PARAMS to be extracted from layout in between the coupling cap and the “remaining trace.” Assume one taps into the Orin module Tx lane-n, the coupling cap will be removed, and Orin module Tx lane-n will be probed at the coupling cap (Orin module side). The S-PARAM extracted from layout must model the remaining trace from the coupling cap to the device pins. A scope used in this DUT setup must be able to fold in real-time filters for convoluting S-PARMS with real-time measurement to model the “remaining trace” real time.

Oscilloscopes

An oscilloscope is used to measure and capture the signals for Tx characterization. It must fulfill data signal bandwidth requirements. The oscilloscope bandwidth shall be above Nyquist frequency. For Gen4 maximum bandwidth must be greater than or equal to 25 GHz and have a minimum sample rate of 64 GS/s. For Gen3 it must be at least 13 GHz and 32 GS/s.

BERT

A Bit Error Rate Tester (BERT) may be used for Rx testing, for example, the Rx_LINK equalizer test. The BERT must be capable of acting as a loop-back initiator to drive the DUT lanes selected for test into loop-back mode with the BERT acting as a link partner using interactive link training.

Cables

It is important when probing to use the lowest loss cables possible. For PCIe data lanes (and REFCLK differential measurement), high-quality SMA cables must be used along with short SMA-SMB cables (when needed). This is to probe the differential data signal taping into a breakout board soldered to the PCB exhibiting an SMA connector. Cables, connectors, and termination such as SMA (male)-SMA (male) cable, SMA (female)-SMP cable, SMP-SMP, SMA male connector to SMP female connector and so on. SMP 50 Ω termination resistors shall be good for 25 GHz or greater.

Probes

Probes are used to connect the oscilloscope and BERT to the test fixture or probing points. Special adapters (breakout boards) and solder tips for probes may be required depending on selected setup. The following probes may be required:

- 2× high Impedance and high-bandwidth probes (single-ended) for REFCLK stand measurements.
- 50 Ω differential probes for REFCLK differential measurement and PCIe Rx and Tx lane characterization.

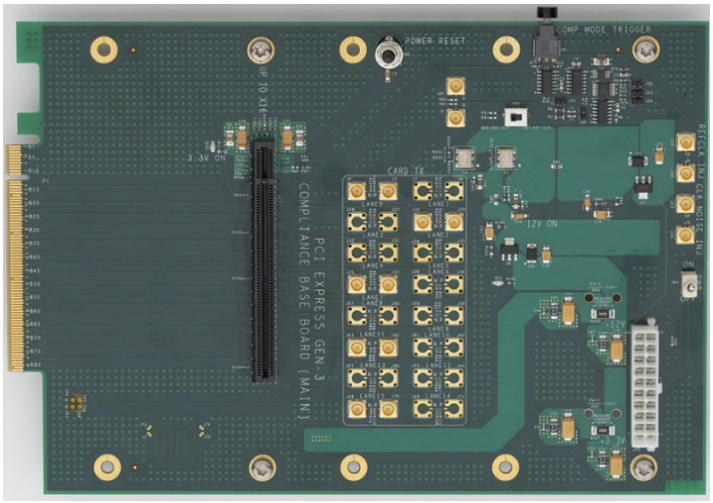
Mode Pulse Generation

For Tx measurement, a 100 MHz and 1 ms pulse must be injected into the corresponding Rx lane-n of the Tx lane-n to be characterized. Each single mode pulse will switch the Tx lane into the subsequent preset. The default Tx preset after power-up will be Gen1. For this purpose, either a PCI-SIG CBB standalone, or a signal generator may be used. Here is a brief overview as to how to use a CBB as mode pulse generator for this purpose:

1. Set clock source to internal. Use internal oscillator to generate pulse. See the area circled in yellow in Figure 2.

2. Connect CBB J5/J85 to Rx lane-n P+ / P- of DUT.
3. Connect ATX power supply to connector.
4. Fix CBB in a stand or holder.
5. Use push button to issue pulse to step through presets. See the area circled in blue in Figure 2.

Figure 2. Use of CBB as a Mode Pulse Generator

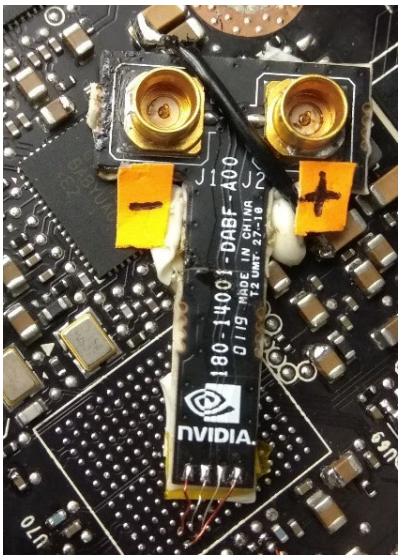


Breakout Boards

NVIDIA uses a proprietary purpose-built breakout board for differential measurement to tap into the solder pads of the devices taken off the board. It may also be used to inject the 100 MHz and 1 ms trigger pulse on Rx lanes to a DUT. Customers are requested to create or purchase an equivalent solution or use probe solder tips. The breakout board is a good example of how to provide connectivity into the DUT.

When using a breakout board, use a breakout channel S-Parameter file used to de-embed the breakout channel when necessary. When using the S-Parameter file, the scope must be capable of convoluting real-time measurement with S-Parameters.

Figure 3. SMA Differential Breakout Board



Software

Use of official compliance test software is recommended, but not required. While manually measuring the signal might be just as effective, it must ultimately pass with the compliance software.

Table 5 contains a list of the recommended test software.

Table 5. Recommended Test Software

Company	Product	Image and Description
PCISIG	Sigtest	Sigtest post processing analysis tool https://www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html?grouping=rdc%20Content%20Types&sort=title:asc
PCISIG	Clock Jitter Tool	Clock jitter tool https://www.intel.com/content/www/us/en/design/technology/high-speed-io/tools.html?grouping=rdc%20Content%20Types&sort=title:asc
Test Equipment Vendor	Scope, BERT software and libraries	Capable Scope and BERT. Dedicated Test Software Package for PCIe testing. See scope vendor for tailored software packages.
Bitifeye	N5990 software	Optional software package Example: https://www.bitifeye.com/download/ Also see: Keysight N5991 PCIe Test Automation Software Platform

Company	Product	Image and Description
NVIDIA	PATCH-A (mandatory)	Patch to OS- PCIe driver to avoid PCIe controller power down for Orin Tx testing for Orin as DUT. Use the patch for the OS release being used. Open a BUG to track PATCH-A release.
NVIDIA	PATCH-B (mandatory for Gen3 Sigtest)	Patch to OS- to disable Orin SSC on RefCLK. In some cases, SSC for the Orin module RefCLK must be disabled for Sigtest measurement. Use the proper patch for the OS release being used.

Setup and Characterization

This section details the setup and characterization for the PCIe compliance testing.

DUT Setup

The DUT setup described here is based on the proprietary breakout board. The DUT setup described hereinafter assumes the use of this breakout board and is an example of how test gear can be connected to PCB probe points with best integrity. In place of breakout boards customers may use other methods, for example using solder tips for probes.

Customers are required to provide their own solution.

Breakout Boards

Breakout board connections described here are for the NVIDIA proprietary solution. The following section describes how to connect the breakout board as a reference example:

The breakout board has four solder tips to connect to the PCB opposite to SMA:

- P+,
- P+GND,
- N-,
- N-GND.

There are two SMA connectors, opposite to tips, to connect to the scope differential probes.

- SMA+
- SMA-

To connect the breakout board to the desired solder pad on a PCB, an AWG38 (0.04” inch) wire may be used for soldering the breakout board tip pads to the + PAD and its closest GND and to the PAD. This is used for PCIe lane, and REFCLK measurement. Keep the wires as short as possible. The shorter the length of the wires used, the better. Ensure that both P and N wires are similar in length to avoid skew.

Use hot melt adhesive for strain relief and fastening the breakout board onto the PCB. This is important to avoid strain or movement on the soldered wire when probing. Choose the hot melt adhesive according to the ambient temperature that the DUT is going to be subjected to. Higher temperature use case will need a high heat resistance glue to be used.

Alternatively, when using solder tips for 50 Ω (differential) probes, follow the same procedure.

REFCLK Measurement and Characterization

Refer to the *Jetson Orin NX Series and Orin Nano Series Product Design Guide* for recommendations and information regarding the use of REFCLK and use of spread NVIDIA Spectrum™ clocking (SSC).

For PCIe controllers acting as and end point (EP), separate reference clocks with no SSC (SRNS) are recommended. Correct PCIe controller configuration is automatically guaranteed when loading the OS (configured for this platform with DUT) when booting. When using Sigtest and clock jitter tools, take SRNS or SRIS requirements into consideration.

Gen3 Sigtest post processing with SSC switched on is not supported yet and the tool cannot process it. Consider the use of PATCH-B (see Table 5) to disable SSC when needed.

The Tx compliance test using PCISIG software Sigtest provides a pass or fail criterion with post processing including REFCLK trace files. In case the mask fails, it may be hard to determine the root cause. Before running Tx compliance testing, it may be useful to characterize REFCLK AC timing to make sure that REFCLK does not compromise Tx compliance masks with excessive jitter.

Note that REFCLK setup for REFCLK standalone characterization is different from REFCLK setup in Tx compliance test.

REFCLK Measurement Probe Selection

For REFCLK standalone characterization NVIDIA recommends using high-impedance probes to replicate the open REFCLK termination with 2 pF termination against GND. For differential standalone measurements, 2x single ended active or a single differential active probe may be considered as best solution.

Pay attention to the different REFCLK setup when running standalone REFCLK characterization compared to REFCLK setup for Tx compliance. When setting up REFCLK with Tx compliance testing, the DUT setup expects a normal test configuration connecting 50 Ω SMA cables to the scope input with 50 Ω termination. For a “CLB-like” setup an additional 2 pF termination to GND may be considered. This means that the REFCLK setup for standalone REFCLK characterization is different from Tx characterization.

For Tx compliance the expectation is that jitter behavior will only show a small difference to the open circuit test. The recommendation is that, if eye opening fails, then capture the clock with high impedance probes (REFCLK setup) to analyze the waveform and exclude possible issues from 50 Ω termination.

In all cases, probes must be calibrated and de-skewed especially for the single-ended probe measurements.

Single-Ended REFCLK AC Measurements

Figure 4 shows a single-ended (SE) setup for REFCLK AC measurements.

Figure 4. SE DUT for REFCLK AC Measurement

The 2× single measurements are for:

- Vcross Max, Vcross Min and Delta
- Vmax and Vmin
- Rise-Fall Matching

For SE measurements 2× high impedance SE probes must be attached to REFCLK-, and REFCLK+. It is using breakout boards with appropriate scope high impedance setup or probe solder pads, which are high impedance probes with solder pads. A 2 pF C_{load} must be applied to each REFCLK-, and RefCLK+ signal pad.

General Setup Considerations

- Turn off Sin(x)/x interpolation.
- For measurements with long captures of clock, maximize real sampling without going into interpolated time sampling.
- For measuring edge information, interpolated time is necessary since less than 1 ns/div usually.
- Probes must be calibrated and de-skewed especially for the single-ended probe measurements.

Rise-Fall Matching

- Set for 1 us/div (1,000 periods). Maximum real-time sampling (not interpolated time).
- Capture REFCLK+ and REFCLK- on two separate channels and save into CSV files (such as data1 and data2).
- Some scopes should automatically generate a CSV for each channel

- Write a script or MATLAB function to find the following number:

$$\text{Rise} - \text{Fall Matching} = \text{Max}\left[\left|\frac{\text{Rise}_{\text{refclk}+} - \text{Fall}_{\text{refclk}-}}{\text{Max}\left[\text{Rise}_{\text{refclk}+}, \text{Fall}_{\text{refclk}-}\right]}\right| * 100\right]$$

The formula essentially means:

Max
- (data1 – data2)/data1 * 100, when data1 > data2
- (data2 – data1)/data2 * 100, when data2 > data1

Vmax and Vmin

- Bring CH1, CH2 to cross each other on the screen.
- Set “No Persistence” in Display menu.
- Go to Measurements → Measurement Setup -->Select CH1--> Amplitude --> Max, Min. Repeat for CH2.

Vcross Max, Min, Delta using Manual Approach

- Bring CH1, CH2 to cross each other on the screen.
- Increase the vertical and the horizontal scale to the maximum.
- Set it to “Infinite Persistence” in Display menu.
- Use two horizontal bars to measure the crossing.
- Note down in Vcross Max, Vcross Min and Vcross Delta (difference between these two values).
- Save as XXX_S1.png file where XXX = PE0, PE1, PE2, depending on the slot that is being characterized.

Vcross Max, Min, Delta with Jitter Application Software

- Use DPOJET or JIT3 (Jitter Advanced) software or equivalent.
- Set Source 1 to REFCLK+ and set for rising and set Source 2 to REFCLK- and set for falling.
- Record max, min, and delta over 80,000+ measurements.
- See specification for: Vmin <Vcross<Vmax, Delta.
- Setup voltage max and min measurements and measure 1000+ measurement samples on each single end.

Differential REFCLK AC Measurements

All other REFCLK AC measurement shall be executed with differential setup (high impedance probes). Use probes with soldering pads to connect scope differential probe to REFCLK+ and REFCLK-. When using breakout boards connect SMA cables from breakout board to probes.

Edge Rate Max and Min, Falling and Rising

- Measured from -150 mV to +150 mV, centered at differential 0. Set scale to see a single rising and falling edge depending on the measurement.
- Use the rise time measurement for rising edge and fall time measurement for falling edge. Set reference levels for the measurement to -150 mV and +150 mV for the range.
- Take more than 1,000 measurements. 0.3/time = V/ns. Use the min and max times for max and min edge rates respectively. See specification for edge rate.

Vih, Vil, Tperiod, % Duty Cycle

- Use the measurement functions for these parameters.
- Take more than 1,000 measurements.
- See specifications for Vih, Vil, Tperiod<10.203 ns, Average Accuracy, and Duty Cycle.

Tstable

Use Min. Neg. Width and Pos. Width, set the mid ref level at -150 mV or +150 mV respectively for the measurement. Alternatively, the trigger level can be set to -150 mV and +150 mV and an infinite persistence measurement can be taken of the minimum for each. Take more than 1,000 measurements. See specification for Tstable.

Tx Characterization DUT Test Setup

For REFCLK, see notes regarding REFCLK characterization. In case Tx test is executed for a PCÍe device (which means that Orin was taken off the PCB) and Orin is providing REFCLK to the device, then use the breakout board to inject compliant REFCLK through appropriate solder pads (Orin side) to the DUT.

For the Tx test setup, the following soldering pads of the removed device must be identified to test DUT Tx lane-n (each Tx lane will be tested separately one by one for each single preset starting with lane-0 with [lane-0 < lane-n < lane-m], where m for lane-m is 0 for x1, 3 for x4 and 7 for x8) and n in [0..m]. Also locate soldering pads for REFCLK+, nearest GND to REFCLK+, REFCLK- and nearest GND to REFCLK-. Solder down breakout boards.

Tx Lane-n+, nearest GND to lane-n+

Tx Lane-n-, nearest GND to lane-n-

} Breakout board #1

Rx Lane-n+, nearest GND to lane-n+

Rx Lane-n-, nearest GND to lane-n-

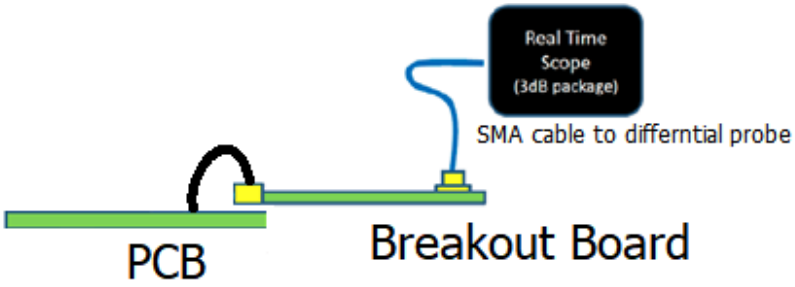
Breakout board #2

RefCLK+, nearest GND to RefCLK+

RefCLK-, nearest GND to RefCLK-

Breakout board #3

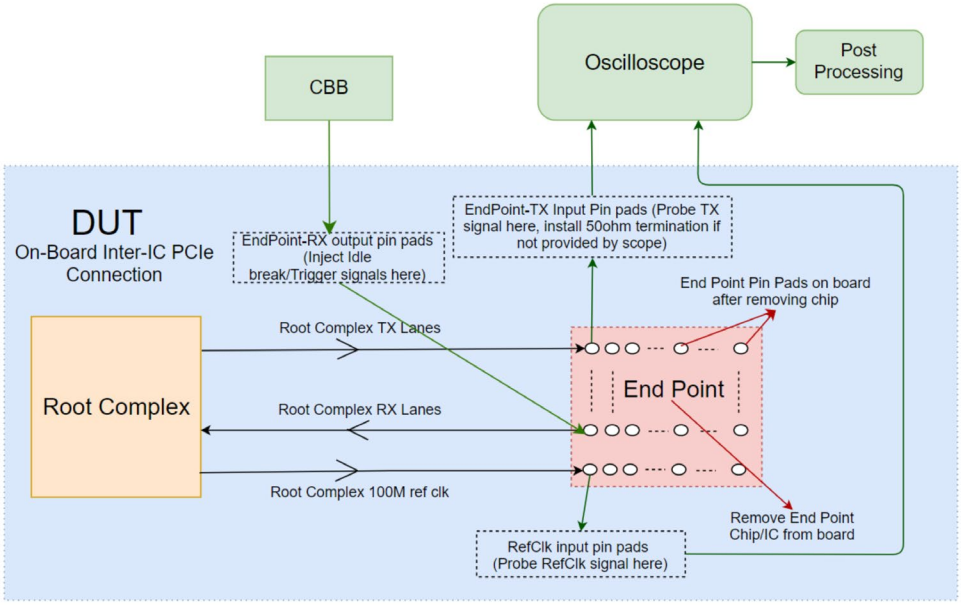
Figure 5. Breakout Board 50 Ω Differential Measurement Use



1. Connect breakout board #1 P+ / P- by SMA to differential probe CH1-CH3 (data).
2. Connect breakout board #3 P+ / P- by SMA to differential probe CH2-CH4 (clock).
3. Connect breakout board #2 P+ / P- by SMA to signal generator or CBB (see Figure 5). When using CBB as pulse source, connect CBB J5/J85 to Rx lane-n P+ / P-. This will inject the pulse used for pattern sequence change (preset) when the toggle push button is pressed. Else, if a pulse generator is used in place of CBB then connect the pulse generator to Rx lane-n.

Figure 6 shows a common clock (CC) configuration.

Figure 6. Orin Probing Diagram with PCIe Device Removed



Tx Test

For the Tx test, the PCIe specification describes a mechanism for testing the electrical characteristics, which relies on a 50 Ω termination on the transmit lane to be tested. Therefore, when the transmit lanes of the device are terminated with a 50 Ω termination, the transmit lanes will automatically be forced into compliance mode. In this setup, the 50 Ω probe termination on Tx lane-n under test will force compliance mode.

Make sure to apply PCIe controller always-on patch (PATCH-A) and apply REFCLK SSC disable patch (PATCH-B) when needed. The patched OS must be flashed before test and then system must boot from flash.

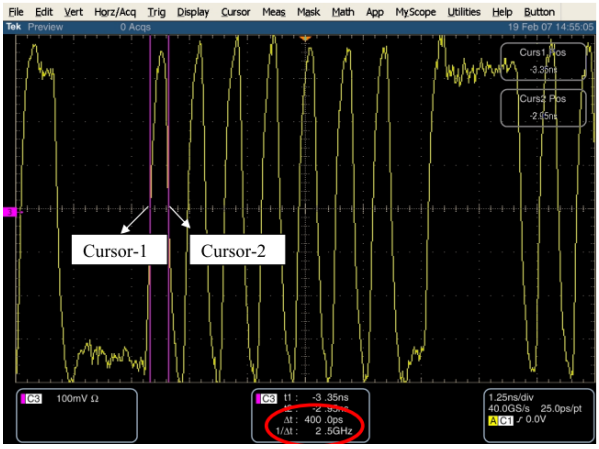
Steps for Gen1 to Gen3 Tx compliance testing are as follows:

1. Make sure wiring as per" Tx Test Setup" is complete.
2. Turn on the power supply powering CBB or turn on pulse generator.
3. Power on DUT, and boot into (patched) OS.
4. Use differential mode on scope, data →CH1-CH3 and CLOCK →CH2-CH4.
5. Adjust the horizontal scale on the scope, so that the data signal differential waveform is clearly visible as shown in Figure 7.

Figure 7. Differential Data Signal Waveform

6. Set scope scale (20 us)/Bandwidth (13 G at least)/memory depth (10 M)/Sample rate (40 G).
7. Device with lane-n under test shall come up in Gen1 preset. Check scope REFCLK and data lanes to make sure that Gen1 preset is achieved. After each new preset, check scope REFCLK and data lanes to make sure that proper presets are achieved.
8. Capture the waveform corresponding to PCIe Gen1, Gen2, and Gen3 for all presets (Gen1-1, Gen2-2, and Gen3-10 presets), move to different PCIe preset by inserting trigger pulse on Rx line. For example, by pressing the CBB toggle button. (first toggle will move from Gen1 to Gen 2-1). Make sure that the user interface numbers meet the following requirements:
   a. Gen1, 10E6 × 400.0 ps = 400.0 μ s
   b. Gen2, 10E6 × 200.0 ps = 200.0 μ s
   c. Gen3, 10E6 × 200.0 ps = 200.0 μ s
   d. Check that the pattern on the scope is intended compliance pattern as specified by the *PCIe Base Specification*. The default the compliance pattern is sent at 2.5 GT/s (initial state with no prior mode change). Use cursors shown in Figure 8 on a pair of adjacent crossover locations to make sure that the user interface reflects the expected preset.

Figure 8. Gen1 Data Signal at 2.5 GT/s Showing User Interface = 400 ps



9. Capture 100 M REFCLK waveform file and store it for post processing. In case spread Spectrum is enabled on REFCLK, then REFCLK shall be captured simultaneously along with data lane on a different channel.
10. Run post processing (for example, by Sigtest) by loading the Tx waveform file and clock file. Once post processing (for example, SIGETST) proves result then a report must be generated. When using Sigtest, it will generate reports by a script.
11. Toggle the button and change compliance pattern sequence and start the capture process again.

> **Caution:** Compliance testing and characterization as described in this application note apply to PCIe Gen1 to Gen3 only. Applying this method to Gen4 may introduce additional noise due to wiring of the breakout boards and running at Gen4 frequencies.
>
> The following steps for Gen 4 Tx compliance testing are for reference only.

Steps for Gen4 Tx compliance testing are as follows and for reference only:

For PCIe Gen4, customers may repeat the steps described Gen1 to Gen3 with the following modifications and additions:

Note that the sequence of modified and additional steps are to fit in with the steps for Gen1 to Gen3.

1. Set scale (12.5 us), bandwidth (25 G at least), memory depth (10 M), and sample rate (80 G).
2. Capture the waveform corresponding to PCIe Gen4. For all Gen4 presets move to different PCIe preset by inserting trigger pulse on Rx line by pressing the CBB toggle button. From default state (Gen1), toggles the DUT into P0 Gen4. Each further toggle moves the DUT on to the next Gen4 preset until P10 Gen4.
3. Make sure that the user interface numbers meet the requirement for Gen4, 2.0 × 10E6 × 62.5 ps = 125.0 μ s

Rx DUT Test Setup

The Rx DUT test setup is like the Tx test setup (See “Tx Characterization DUT Test Setup” section).

1. Connect breakout board #1 P+ / P- by SMA to BERT input (DUT-Tx to BERT INPUT)
2. Connect breakout board #3 P+ / P- by SMA to Bert output (DUT-Rx to BERT OUTPUT)
3. If required: Connect breakout board #2 P+ / P- via SMA to BERT REFCLK input.

Rx Tests

This section describes the Rx tests for compliance testing.

Protocol-Aware BERT

For the Rx test, a protocol-aware test gear is required. Typically, it requires the use of a specialized Bit Error Rate Tester (BERT) along with specialized protocol software and libraries. BERTs capable of PCIe Rx testing are available from test equipment providers such as Teledyne, Keysight, or Tektronix.

The general steps are as follows:

1. BERT drives lane-n state under test into loop-back (Rx -> Tx) through adaptive link training.
2. Performing link equalization
3. Configure and pick impairment signal
4. Auto calibrate stress impairments
5. Run BERT measurements

Since Rx testing through BERT is an involved procedure, NVIDIA recommends following the respective u’er's guide of the test equipment provider for detailed steps through the procedure. As an example, refer to the *Keysight N5991 PCIe Test Automation Software Platform User’s Guide* available from BitifEye / Keysight describing the setup and procedure.

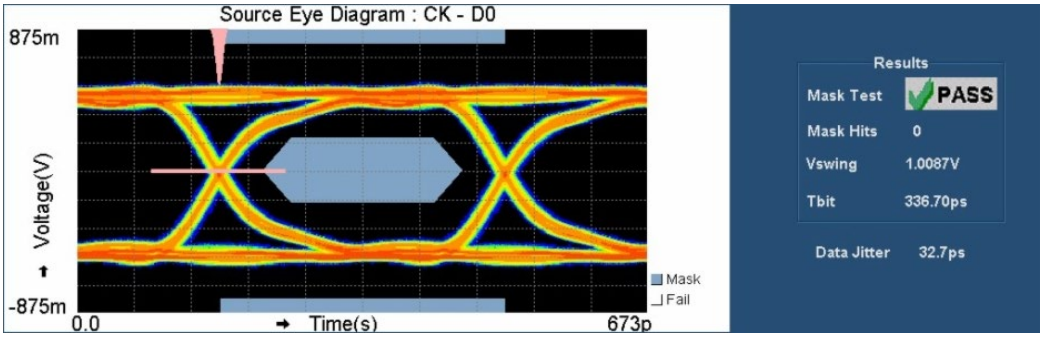
HDMI Tuning Guide

This chapter describes the registers and steps needed to tune the HDMI signals output from the Orin module.

To meet HDMI compliance, tuning may be required to adjust the TMDS signal such that the voltage swing is close to 500 mV ± 100 mV single-ended, or 1,000 mV ± 200 mV differentially. This is to ensure that the signal integrity is clean, meets the HDMI specifications, and the device is optimized for low power consumption.

Note: Before any tuning, scope and probes must be calibrated. Refer to the documentation for your scope and probe for instructions on how to calibrate.

Figure 9. Source Eye Diagram: CK-D0



Abbreviations and Definitions

Table 6 lists the abbreviations that may be used throughout this chapter and their definitions.

Table 6. Abbreviations and Definitions

Abbreviation	Definition
CTS	Compliance Test Specification
DUT	Device Under Test
EMI	Electromagnetic Interference

Abbreviation	Definition
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
PVT	Process, Voltage, and Temperature
RF	Radio Frequency
Sink	Any type of receiver, such as a display or panel
SOR	Serial Output Resource – Module naming referring to the HDMI block
Source	Any type of transmitter, such as Orin
TMDS	Transition-Minimized Differential Signaling

Required Equipment

There are many tools currently available to perform the HDMI tuning. The following components are required:

- Test fixture
- Oscilloscope
- Probes
- DC power supply
- Software
  - HDMI compliance software
  - Tools to access register space in Orin

The following subsections list some of the acceptable equipment that may be used.

Note: The items highlighted with green in the following sections are the tools that NVIDIA used for validation and tuning. This guide will refer to those tools specifically for the rest of this chapter.

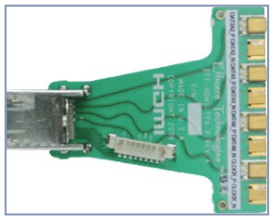
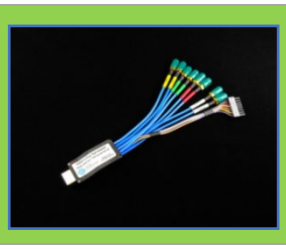
Test Fixture

Test fixtures are used to connect the probes to the output of the HDMI interface. The following example fixtures listed use the Type-A interface for HDMI 1.4b compliance. Fixtures of different interface types are available and are recommended instead of using adapters to convert the interface Type.

For HDMI 2.0 compliance, ensure that the test fixture can support the higher bitrate with minimal insertion loss.

The fixture selected must have SMA interconnects to avoid impedance mismatches due to discontinuities.

Table 7. Partial List of Acceptable HDMI Test Fixtures Type A

Efficere	EFF-HDMI-TPA-P	
Agilent	N1080A	
Wilder Tech	HDMI-TPA-P	

Oscilloscope

The scope is used to display and measure the signals. The HDMI 1.4 specification requires that the scope has at least 8 GHz of bandwidth and a sampling rate of at least 10 GS/s if the pixel clock is equal to or less than 165 MHz, or sampling rate of at least 20 GS/s if the pixel clock is greater than 165 MHz.

Table 8. Partial List of Acceptable Oscilloscopes for HDMI 1.4 Tuning

Tektronix	TDS6804B or better	
Agilent	DSO80000B or better	

For HDMI 2.0, a scope with at least 16 GHz of bandwidth is recommended.

Table 9. Partial List of Acceptable Oscilloscopes for HDMI 2.0 Tuning

Tektronix	DPO/MSO 70,000 series 16 GHz or better	
Agilent	Infiniium 90,000 series 16 GHz or better	

For HDMI 2.1, a scope with at least 21 GHz of bandwidth is recommended.

Table 10. Partial List of Acceptable Oscilloscopes for HDMI 2.1 Tuning

Keysight	V, Z, and UXR Series Minimum 20 GHz bandwidth	
Tektronix	DPO70000SX/DX Series Bandwidth ≥ 20 GHz	

Probes

Probes are used to connect the scope to the test fixture. The probes must have at least 8 GHz of bandwidth for HDMI 1.4b testing and at least 12 GHz of bandwidth for HDMI 2.0 testing.

At least two probes are required for tuning. However, four probes are ideal.

Untested lanes must be terminated appropriately. See the “DC Power Supply” section for details.

Table 11. Partial List of Acceptable Probes

Tektronix	P7313SMA	
Agilent	1169A Requires Agilent N5380A	
Agilent	N5380A Used with Agilent 1169A	

Table 12. Partial List of Acceptable Probes for HDMI 2.1

Keysight	N7003A (probe Amp) 20 GHz	
Keysight	N544A (probe head)	
Tektronix	P7625 25 GHz	

DC Power Supply

Any power supply that can supply a constant voltage of 3.3V is needed to terminate the HDMI signals. Refer to the probe's instruction manual on how to supply this termination voltage to the probes.

Note: All untested lanes must be terminated to 3.3V using 50 Ω terminators. Irrespective of the tools used, it is important to make sure that they are calibrated and meet industry standards to obtain accurate measurements.

On Tektronix scopes, the probe and scope can be configured such that the scope can internally apply 3.3V to the probes. This is acceptable for compliance testing.

Software

This section describes the software used for HDMI tuning.

Compliance Test Software

NVIDIA recommends that the official compliance test software is used to ensure accurate results. Although manually measuring the signal may be as effective, it must ultimately pass with the compliance software at the compliance house.

Table 13. Partial List of Acceptable Test Software

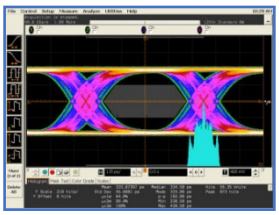
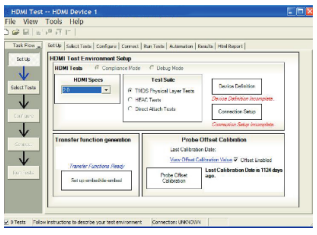
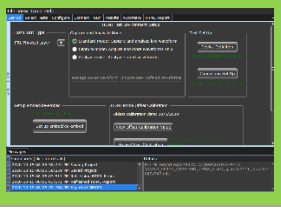
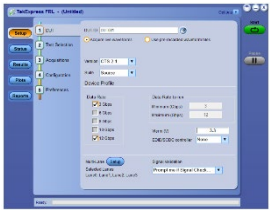
HDMI 1.4b Testing		HDMI 2.0 Testing	
Tektronix TDSHT3 or later		TekExpress HDM or later	
Agilent N5399A or later		Agilent N5399C or later	

Table 14. Partial List of Acceptable Test Software for HDMI 2.1

HDMI 1.4b Testing	HDMI 2.1 Testing	
Keysight	D9021HDMC HDMI Electrical	
Tektronix	TekExpress FRL	

Software Tools

Consult your software team or contact your NVIDIA representative for assistance with software tools to access the register space in Orin.

Method for Tuning

Tuning is done by running the eye diagram tests on each of the data lanes while shmoo'ing the applicable registers. The objective is to keep the differential voltage swing as close to 1000 mV as possible, while providing the eye diagram enough margin to meet HDMI specifications.

Procedures

Calibrate the scope and probes before you begin. Refer to your scope and probe user manuals for details on how to calibrate.

DUT

This guide does not cover setup of HDMI at any specific resolution. Work with your software team and NVIDIA representative to prepare the DUT for testing. Following are the general steps to set up the HDMI connection.

1. Disable Hot Plug Detect: The driver or OS may disable HDMI output if it detects the panel being disconnected. Try the following methods to prevent that:
   a. **Method #1:** Disable the HPD interrupt through software by setting the HPD pin to TRISTATE.

   b. **Method #2:** Disconnect the HPD circuit from the HDMI connector, manually rework HPD circuit to a desired voltage level to input to Orin to make the software consider HDMI is still connected.
      i. Refer to the carrier I/O board schematics for how to do that. If this method is chosen, the circuit must be restored before performing the HDMI certification tests.
2. Configure the DUT to drive HDMI at the supported resolutions:
   a. 480p (27 MHz)
   b. 720p (74.25 MHz)
   c. 1080p (148.5 MHz)
   d. 2160p/30 (297 MHz)
   e. 2160p/60 (594 MHz)
3. Attach the test fixture to the DUT.
4. Attach the probe-ends to the test fixture, and properly connect the termination voltage to the probes. Untested lanes must be properly terminated.
5. Attach the probes to the scope.

Note: For using an HDMI converter (to GMSL/FPD link/MIPI, and so on) design on board, HDMI CTS is not required. To check the HDMI signal quality from Orin, probe the HDMI signals closest to the input of the HDMI converter to confirm if the signals meet the HDMI source electrical specification or HDMI converter's input electrical specification.

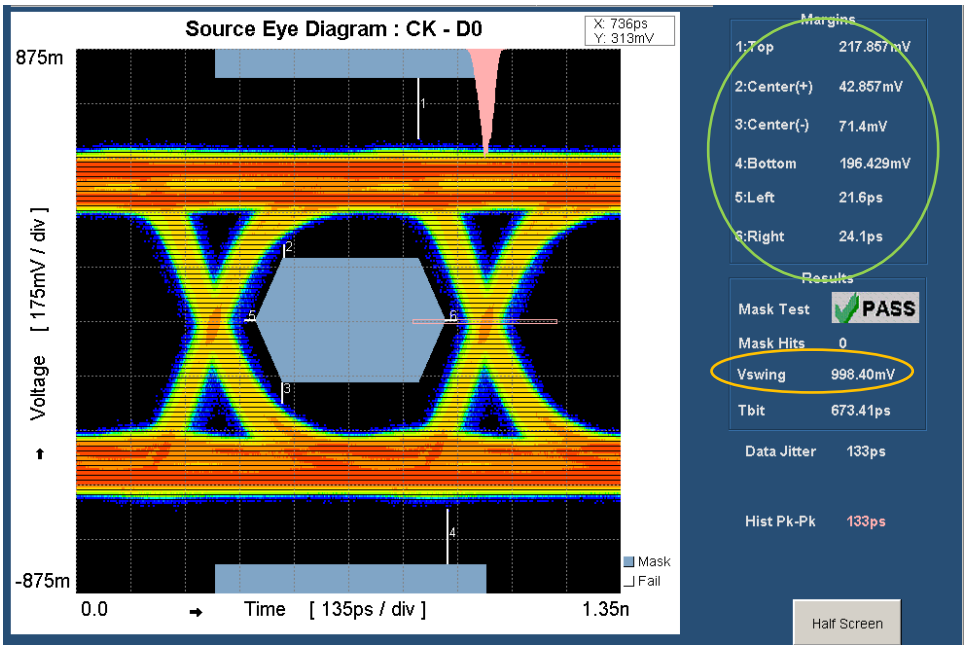
Oscilloscope

1. Ensure that the probes are using the termination voltage of 3.3V.
2. Start the HDMI compliance software.
3. Set up the HDMI compliance software to take the Eye Diagram and configure the probes to the proper clock and data assignments.
4. Run the eye diagram test.
5. Check the voltage swing and margin result (see Figure 10).
6. See Section: Registers note the internal termination, drive strengths, and pre-emphasis settings.
7. Repeat for all data lanes, using different register settings, at all supported resolutions.

Tips:

- When shmoo'ing drive strengths or pre-emphasis, keep the same value across each data lane. The HDMI pads for each of the data pairs and the clock are the same and should have very minor variation.
- Since HDMI clock has fewer transitions than data, its settings can be weaker than the data lanes. This can save some power and lower possible noise or EMI.

Figure 10. Voltage Swing and Margin Results



Objectives

While there is no margin specification, a good rule of thumb is to provide:

- At least 40 mV of margin above and below the eye mask
- Voltage swing of around 1,000 mV
- Find settings for:
  - 480p
  - 720p
  - 1080p
  - 2160p/30
  - 2160p/60

Tips:

- Lower drive strength, I/O peak current, and pre-emphasis settings will lower the power consumption.
- The stronger the termination, more current is needed and therefore a higher power consumption.
- Fast rising and falling edges will contribute to increased EMI.

Voltage Swing Target

This guide targets a differential voltage swing of 1,000 mV.

The target can be lowered to help reduce EMI and RF related issues.

> **Caution:** Note that if the user lowers the differential voltage swing target, the user assumes complete responsibility for issues or consequences arising as a result. In addition, the user must test random parts to ensure HDMI compliance with the new differential voltage settings.

Slew Rate

The **NV_PDISP_SOR_PLL_SPARE_0_0** register controls slew rate to reduce EMI at the expense of eye height, especially for the 297MHz and 594MHz cases. Setting fields in this register to non-zero values enables the slew rate control, with larger values reducing the slew rate further. See Table 15.

By default, the setting in this register is all 0s, which disables slew rate control and results in the sharpest waveform.

To enable slew rate control, set both registers: **NV_PDISP_SOR_LANE_PREEMPHASIS_0** and **NV_PDISP_SOR_PRESHOOT 0** to 0x00000000.

Registers

The Serial Output Resource (SOR) module can be configured to support HDMI or DisplayPort (DP) technology. The Orin module has one instance of the SOR module on the **HDMI_DP2** pins.

Table 15. Orin SOR Registers for HDMI

Register Name	Bit Fields	Description	Notes
NV_PDISP_SOR_LANE_DRIVE_CURRENT_0: Address 0x1380c118			
LANE2_DP_LANE0	07:00	Drive Strength controls for Lane 2	Used to set transmitter main output drive level for each of the four lanes.
LANE1_DP_LANE1	15:08	Drive Strength controls for Lane 1	
LANE0_DP_LANE2	23:16	Drive Strength controls for Lane 0	
LANE3_DP_LANE3	31:24	Drive Strength controls for Clock	
NV_PDISP_SOR_LANE_PREEMPHASIS_0: Address 0x1380c120			
LANE2_DP_LANE0	07:00	Pre-Emphasis controls for Lane 2	
LANE1_DP_LANE1	15:08	Pre-Emphasis controls for Lane 1	
LANE0_DP_LANE2	23:16	Pre-Emphasis controls for Lane 0	
LANE3_DP_LANE3	31:24	Pre-Emphasis controls for Clock	
NV_PDISP_SOR_PRESHOOT 0: Address 0x1380c14c			

Register Name	Bit Fields	Description	Notes
LANE2_DP_LANE0	07:00	Preshoot controls for Lane 2	
LANE1_DP_LANE1	15:08	Preshoot controls for Lane 1	
LANE0_DP_LANE2	23:16	Preshoot controls for Lane 0	
LANE3_DP_LANE3	31:24	Preshoot controls for Clock	
NV_PDISP_SOR_PLL_SPARE_0_0: Address 0x1380c038			
RESERVED	31:16	Reserved	
SPARE3	15:12	Bit 15 not used, set to 0 Bits 14:12 control slew rate for Clock 0'b000 = slew rate control disabled / sharpest waveform (default) 0'b001 = fastest slew rate delay enabled … 0'b111 = slowest slew rate delay enabled	Set NV_PDISP_SOR_LANE_PREEMPHASIS_0 = 0 and NV_PDISP_SOR_PRESHOOT 0 = 0 when slew rate control is enabled
SPARE2	11:08	Bit 11 not used, set to 0 Bits 10:08 control slew rate for Lane 2 0'b000 = slew rate control disabled / sharpest waveform (default) 0'b001 = fastest slew rate delay enabled … 0'b111 = slowest slew rate delay enabled	
SPARE1	07:04	Bit 07 not used, set to 0 Bits 06:04 control slew rate for Lane 1 0'b000 = slew rate control disabled / sharpest waveform (default) 0'b001 = fastest slew rate delay enabled … 0'b111 = slowest slew rate delay enabled	
SPARE0	03:00	Bit 03 not used, set to 0 Bits 02:00 control slew rate for Lane 0 0'b000 = slew rate control disabled / sharpest waveform (default) 0'b001 = fastest slew rate delay enabled … 0'b111 = slowest slew rate delay enabled	

Final Steps

This section details the final steps for HDMI tuning.

Sanity Check

After tuning is completed, the settings should be sanity-checked to make sure they do not violate any other parts of the HDMI specifications, and there is enough margin.

The DUT should go through the full set of electrical tests outlined in the *HDMI Compliance Test Specifications (CTS)* document to ensure that the DUT can pass HDMI certification.

If there are any failures, the settings must be tuned again until there is a passing result.

Note: : Higher power consumption is expected if the new settings are stronger than the default settings. Stronger settings are required due to, but not limited to, longer traces, EMI chokes on the signal paths, or signal integrity issues.

Updating the Software

After the tuned settings have been verified, they must be updated into the OS or the driver. Contact the appropriate software team, or your NVIDIA representative to update new tuned settings.

- The 480p settings apply to pixel clock resolutions ≤ 54 MHz
- The 720p settings apply to pixel clock resolutions between > 54 MHz to ≤ 111 MHz
- The 1080p settings apply to pixel clock resolutions between > 111 MHz to ≤ 223 MHz
- The 2160p/30 settings apply to pixel clock resolutions between > 223 MHz to ≤ 300 MHz
- The 2160p/60 settings apply to pixel clock resolutions between > 301 MHz to ≤ 600 MHz

Note: Ranges can be adjusted according to design and use-cases. More ranges can also be defined if proper tuning and software implementation is performed.

Final Check

After the settings have been updated in the driver, you must verify that the new tuned settings are really applied to each of the target resolutions.

A visual checkout is recommended as well. Connect the DUT to an HDMI panel and visually check that there is no corruption at any of the supported HDMI resolutions.

DisplayPort and Embedded DisplayPort Tuning Guide

This chapter describes the registers and procedure to tune the VESA® DisplayPort™ (DP) output and Embedded DisplayPort (eDP) in the Orin module.

DisplayPort is a video interface using AC-coupled signals to transmit serialized data to a single display sink, such as monitors. The eDP interface is used for internal connections to drive smaller sinks such as panels or embedded displays.

In addition to the standard DP data rates (RBR, HBR, HBR2, and HBR3) and voltage levels (400 mV, 600 mV, 800 mV, and 1,200 mV), eDP also supports four other intermediate bit rates and lower, optional, voltage swings below 400 mV.

Since there is no compliance specification for the additional bit rates and lower voltage levels supported in eDP, this guide only covers the standard rates and voltage levels using the *DP 1.4a Compliance Test Specification* (CTS). The concepts can still be applied for the other bit rates and voltage levels.

Tuning is needed to make sure that the DP interface can meet the specification for each of the different combinations of voltage and frequency outputs, while minimizing power consumption.

Design choices such as, but not limited to, long routing and layer transitions, can heavily affect the signal integrity, and require some adjustments to overcome the loss.

Abbreviations and Definitions

Table 16 lists the abbreviations that may be used throughout this chapter and their definitions.

Table 16. Abbreviations and Definitions

Abbreviation	Definition
CTS	Compliance Test Specification
DP	DisplayPort
DUT	Device Under Test

Abbreviation	Definition
eDP	Embedded DisplayPort
HBR	High Bit Rate (2.7 Gbps)
HBR2	High Bit Rate 2 (5.4 Gbps)
HBR3	High Bit Rate 3 (8.1 Gbps)
Link Training	Establishing a link between source and sink before normal operation
RBR	Reduced Bit Rate (1.62 Gbps)
Sink	Any type of receiver, such as a display or panel
SOR	Serial Output Resource. Module naming referring to the DP and eDP block
Source	Any type of transmitter, such as Orin
SSC	Spread Spectrum Clock, will reduce EMI

Required Equipment

The following hardware and software are required:

- Hardware
  - DP Plug Test Fixture, corresponding to the plug type
  - Oscilloscope and Probes
  - Unigraf DPR-100 DisplayPort Reference Sink or UCD-400 DP 1.4a – HBR3 8K Generator & Analyzer
- Software
  - DisplayPort Compliance Test Software
  - NVIDIA Orin DisplayPort Driver for AUX channel automation

Test Fixtures

Test fixtures connect the probes to the outputs of the Serial Output Resource (SOR) of the DUT. NVIDIA recommends that a native fixture be selected and that no adapters be used between the DP connector and the DP test fixture, since adapters will heavily affect the signal integrity.

List of test fixture vendors:

- WilderTech
- VPrime
- Keysight

Oscilloscope and Probes

The oscilloscope and probes are used to measure the signal electrically. The equipment must be capable of accurately measuring the maximum bitrate supported by the DUT, up to 8.1 Gbps (HBR3).

The following are examples of testing solutions:

- Tektronix:
  https://www.tek.com/displayport

  https://www.tek.com/datasheet/displayport-14-and-type-c-compliance-debug-solution

  https://www.tek.com/oscilloscope/dpo70000-mso70000

  https://www.tek.com/oscilloscope/dpo70000sx

  https://www.tek.com/datasheet/displayport%28tm%29-14-sink-calibration-and-test-software-%28dp-sink-bsx-dp-sink%29c
- Keysight:
  https://www.keysight.com/us/en/product/D9040DPPC/displayport-1-4-compliance-validation-test-software.html

  https://literature.cdn.keysight.com/litweb/pdf/5991-1784EN.pdf?id=2295383
- Unigraf:
  https://www.unigraf.fi/product/dpr-100-displayport-reference-sink/

  https://www.unigraf.fi/product/ucd-400-dp-1-4-test-device/

Unigraf DPR-100 or UCD-400

The Unigraf DPR-100 DisplayPort Reference Sink or UCD-400 DP 1.4a – HBR3 8K Generator & Analyzer act as a DP AUX channel controller that connects between the Oscilloscope and the DUT to allow for DPCD-based automated compliance testing. The Oscilloscope passes the requested parameters over USB to the DPR-100 or UCD-400, which sends the parameters to the Orin DP driver through DPCD commands over the DP AUX bus by the test fixture.

Refer to the test equipment documentation and dealer for more information.

Software

Only compliance test software should be used to guarantee an accurate result for compliance. The NVIDIA Orin DisplayPort driver supports AUX channel automation with the Unigraf DPR and UCD-400 to help make testing hands free.

Debug tools to access the Orin register space are necessary to fine-tune the settings.

Contact the test equipment dealer directly for more information.

Method for Tuning

There are several settings in the DisplayPort PHY to tune the output to meet the specifications in the *DP Compliance Test Specification* (CTS). The subsequent sections in this chapter describe the major controls to tune for characterization. Tuning consists of

adjusting the settings to meet each voltage swing, pre-emphasis, and maximum differential voltage test for each driver configuration.

Drive Strength

Drive strength controls the amount of drive current of each of the four lanes and can be configured individually, affecting the overall voltage swing. This control has higher priority over pre-emphasis. Meaning if the settings are maxed out, there will be no current drivers for the other controls.

To save power, this setting can be reduced until it can pass with sufficient margin, roughly 20 to 30%.

Pre-Emphasis

Pre-emphasis controls affect the voltage swing of the transition bit. There must be distinct levels of pre-emphasis to meet specifications. Increasing pre-emphasis also affects non-transition bits, effectively lowering the voltage swing of the non-transition bits.

To save power, this setting can be reduced until it can pass with sufficient margin; roughly 20-30%.

Post Cursor2

Post Cursor2 is deprecated and should always be set to 0.

Procedures

Before proceeding with the tuning procedure, the scope and probes must be calibrated. Refer to your vendor-specific scope and probe user manuals for details on how to calibrate. The following procedure uses the Unigraf DPR-100 AUX controller for automation.

DUT

Configure the DUT to output the appropriate output configuration, such as bit rate, swing levels, and test patterns. Then connect the test fixture to the DUT and the test fixture to probes to the scope. Any untested lanes should be terminated with 50 Ω to GND.

Oscilloscope and AUX Channel Controller

After calibration, initialize the compliance test software and configure it for all the modes supported by the DUT. Set up the compliance test software to run automation by choosing "UnigrafDPTC." Refer to the test equipment documentation and dealer for more information for the automation setup.

Objectives

Settings for drive strength and pre-emphasis must be found for the output configurations described in Table 17 and Table 18.

DisplayPort

The tuned settings must work across all bit rates supported by the DUT: RBR, HBR, and HBR2 (optional), and HBR3 (optional).

Table 17. DisplayPort Configurations

Drive Level	Pre-Emphasis Level	Post Cursor2
400 mV	0.0 dB	0
400 mV	3.5 dB	0
400 mV	6.0 dB	0
400 mV	9.5 dB	0

Drive Level	Pre-Emphasis Level	Post Cursor2
600 mV	0.0 dB	0
600 mV	3.5 dB	0
600 mV	6.0dB	0

Drive Level	Pre-Emphasis Level	Post Cursor2
800 mV	0.0 dB	0
800 mV	3.5 dB	0

Drive Level	Pre-Emphasis Level	Post Cursor2
1,200 mV	0.0 dB	0

Embedded DisplayPort

The settings in Table 18 are required for fast link training. Since there is no specification for the other bit rates or voltage levels, this guide will not cover them.

Table 18. Embedded DisplayPort Configurations

Bit Rate	Drive Level	Pre-Emphasis Level	Post Cursor2 Level
RBR	400 mV	0.0 dB	0
HBR	400 mV	0.0 dB	0
HBR2	400 mV	0.0 dB	0

Registers

The Serial Output Resource (SOR) module can be configured to support HDMI or DisplayPort technology. The Orin module has one instance of the SOR module on the **HDMI_DP2** pins.

Table 19. Orin SOR Registers for DisplayPort

Register Name	Bit Fields	Description	Notes
NV_PDISP_SOR_LANE_DRIVE_CURRENT_0: Address 0x1380c118			
LANE2_DP_LANE0	07:00	Drive Strength Controls for Lane 0	Used to set transmitter main output drive level for each of the four lanes.
LANE1_DP_LANE1	15:08	Drive Strength Controls for Lane 1	
LANE0_DP_LANE2	23:16	Drive Strength Controls for Lane 2	
LANE3_DP_LANE3	31:24	Drive Strength Controls for Lane 3	
NV_PDISP_SOR_LANE_PREEMPHASIS_0: Address 0x1380c120			
LANE2_DP_LANE0	07:00	Pre-Emphasis Controls for Lane 0	
LANE1_DP_LANE1	15:08	Pre-Emphasis Controls for Lane 1	
LANE0_DP_LANE2	23:16	Pre-Emphasis Controls for Lane 2	
LANE3_DP_LANE3	31:24	Pre-Emphasis Controls for Lane 3	

Register Name	Bit Fields	Description	Notes
NV_PDISP_SOR_DP_PADCTL0_0: Address 0x1380c130			
TX_PU_LINK_VALUE	11:08	TX common mode pulls up by % of PLL_VDD - IO_VDD. 0'b0000 -> 0% 0'b0001 -> 10% 0'b0010 -> 20% 0'b0011 -> 30% 0'b0100 -> 40% 0'b0101 -> 50% 0'b0110 -> 60% 0'b0111 -> 70% 0'b1000 -> 80% 0'b1001 -> 90% 0'b1010 -> 100%	Configure the TX pull-up drive strength separately for each link of connected SOR.
TX_PU	22:22	Pull-up current sources 0'b0 = Disable 0'b1 = Enable	Configure the TX pull-up current source separately for each link of connected SOR.

Final Steps

This section describes the final steps for DP and eDP tuning.

Sanity Check

After tuning is completed, the settings should be sanity-checked to make sure they do not violate any other parts of the DisplayPort specifications and that there is a comfortable amount of margin based on the user's analysis.

The DUT should go through the battery of electrical tests outlined in the DP CTS document to ensure that the DUT will pass DP certification.

If there are any failures, the settings must be tuned again until there is a passing result.

Updating the Software

After the tuned settings have been verified, they must be updated in the OS or the driver.

Final Check

After the settings have been updated in the driver, verify that the tuned settings are applied for each of the requested modes.

A visual check-out is recommended as well. Connect the DUT to a DP or eDP panel and visually verify that there is no corruption at any of the supported bitrates.

Ethernet Compliance Test Guide

This chapter serves as the high-level guide to compliance testing of the 1000Base-T interface in NVIDIA Jetson Orin NX series and Jetson Orin Nano series. The Orin NX/Orin Nano modules have been tested for specification compliance; therefore, no tuning will be required if customer designs follow the routing guidelines published in our design guides.

Ethernet Compliance Testing

The IEEE Standard for Ethernet defined by IEEE 802.3ab provides the compliance criteria and test descriptions for 1000Base-T. Customers should refer to the document for a high-level overview of the tests that are performed to check the compliance criteria. Depending on the brand of equipment being used for the test, customers can then refer to the manufacturer's documentation for step-by-step procedure to perform the test.

Tools

Mdio-tool is a generic tool which can be used to access the PHY registers from the Linux command line. It can be downloaded and compiled from the following location:

https://github.com/PieVo/mdio-tool

Note: The original makefile is for cross-compilation, therefore it can be built directly on the device through the command "gcc -o mdio-tool mdio-tool.c"

Placing Orin NX/Orin Nano in Compliance Mode

The Orin NX and Orin Nano modules, both integrate a Realtek RTL8111HNI Gigabit Ethernet PHY. Therefore, to perform compliance testing on the Orin NX/Orin Nano, customers will need to contact Realtek to obtain documentation on how to access the internal registers.

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